Sub-MMW Substrate Integrate Waveguide Filter on Silicon Substrate

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***Abstract*- This paper presents a novel sub-MMW substrate integrated waveguide (SIW) filter based on IBM 130-nm CMOS technology. It researches the basic problem such as construct of waveguide and resonator, transition between the substrate integrated waveguide and the micro-strip, and present a filter centered at 400GHz. Simulation results support the design idea. It shows the filter has a good performance.**

I. Introduction

Some advance on sub-MMW CMOS technology [1][2] has drawn the attention in recent years. Although the circuits in Ref [1][2] with output frequency 410GHz was realized by push-push configuration, it successfully proved CMOS technology can be an inexpensive and useful terahertz technology. The progress of key device toward sub-MMW has been made in the Ref [1][2]. In future active devices and passive elements by CMOS will be a research focus. This paper proposed a novel sub-MMW filter by utilizing SIW technology [3][4] on the CMOS technology.

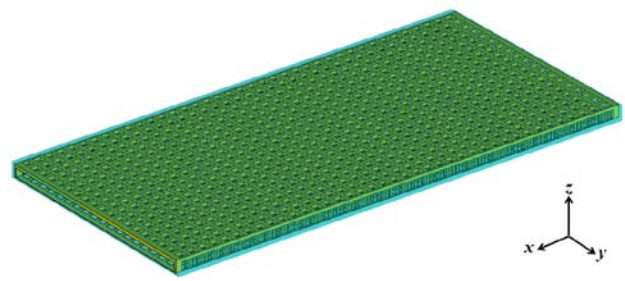
II. Sub-MMW Filter

A. Substrate integrated waveguide

In the CMOS substrate, there can't exits continuous metallic foil with large size due to the limitation of CMOS technology rules. So the method used in traditional substrate integrated waveguide was used again. Simply speak SIW used a metallic foil filled with hole or slot to replace the continuous metallic. If the size of hole or slot is much less than the wavelength, the foil can be equivalent to the continuous foil, although there may be some effects due to the discontinuity. The side wall of waveguide is constructed by rows of metallic via, same as traditional substrate integrated waveguide. Of course the distance between adjacent via should be much less than wavelength.

Fig.1(a) shows a model of SIW on IBM 130nm CMOS substrate. It utilized the substrates between metallic layer MA and LY. On the MA and LY layer, a period structure has been designed. The cell of the structure is square block $15\times 15\mu m^2$. A square hole with size $10\times 10\mu m^2$ was place in the center of the cell. This makes a metallic ratio 55.6% which can easily fulfill the rules. According the relative dielectric constant 4.15 of substrate, width of waveguide is chose 280μm which is suit for a filter centered at frequency about 400GHz.

According the Fig.1 (b), although the hole size is approach the thickness of substrate, the dominant mode TE10 can work in this waveguide. The S parameters in Fig.1 (c) also proved this point. It shows good transmission and matching. The S_{21} approaches 0 dB in the whole band even assign open condition (except XZ plane) to the other boundary.



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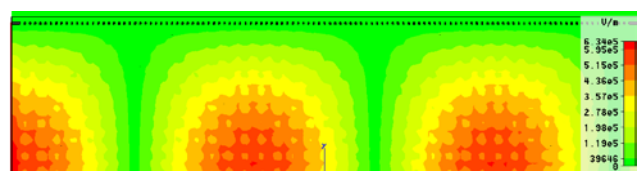

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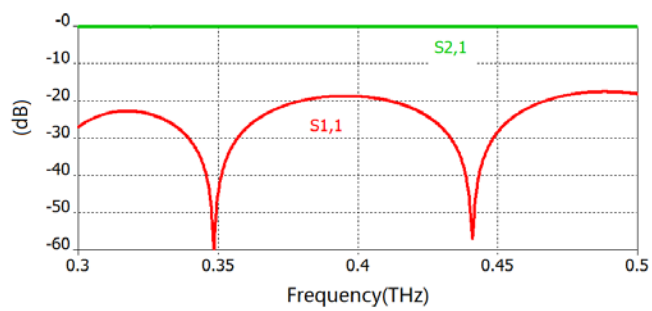


(c)

Fig.1 Substrate integrated waveguide (a) waveguide model (b) field distribution of TE_{10} mode @400GHz (on XY plane, half of the waveguide, with the XZ plane are assigned perfect magnetic conductor.) (c) simulated S parameters

Besides, the extracted phase constant at 400GHz from the simulated results is higher about 5% than the one of solid waveguide with same width. This shows the slight effect of the period structure. The estimation on this difference is important for the design. Because the complexity of some

large element with similar structure will leads it can't be simulated on common computer. Sometimes it need replace or partly replace the element with solid waveguide or cavity. Same method has been used in the traditional SIW design. In their solid walls are usually replace the rows of via to simplify the design.

It has been found that the structure under the LY layer has some uncertain effect on the performance. That may be due to the hole size on LY layer is great but the thickness of LY is thin.

B. Transition

Although transition has been designed according the same method used in traditional substrate integrated waveguide technology, there has shown some difference. Traditional SIW element usually has very thin metallic foil covered on relatively thick substrate. So on traditional SIW technology the rectangular transition is a popular choice due to the simple design and broadband performance. But according the parameters of CMOS substrate, the width of waveguide is much great than the one of micro-strip with a standard impedance, for example, 50 ohm. So the triangular transition can't give well matching even with a very long length.

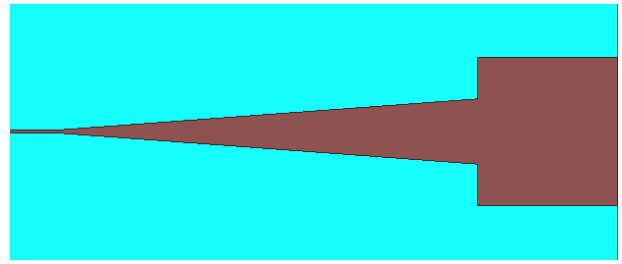
The triangular transition has been compared to the multisection impedance transformers based on the IBM 130nm CMOS substrate. Fig. 2-3 show the simulated results of transitions around 200GHz. According Fig.2, the matching of triangular transition can hardly be view as a good result even with excessive length which reached 1.6mm. On the contrary, a 3 sections impedance transformer just with length 0.603mm has a S_{11} lower than -20dB in fraction bandwidth 38% which is enough for a filter measurement. Besides, rectangular shape is much convenient when plot the layout of chip.

Due to the decreasing of waveguide width as frequency increasing, transformer with fewer sections can give a well matching. Around 400 GHz, 2-sections transformers may fulfill the requirement.

C. Resonator on Chip

A square resonant cavity filled with dielectric was firstly constructed on the chip, same as the process of SIW constructing on CMOS substrate.

Because the design rules require that the ratio of metal area to dielectric area must fall in a given range. So the cavity has been designed as shown in fig.4. Side wall is constructed by rows of via, the upper and lower metallic layer of cavity is a period contracture. For convenient, period structure has been designed being same to the SIW on chip. The dielectric layer utilized the whole layer between the MA layer and the LY layer. In this cavity, the dominant mode TE101 has been found by eigen-mode simulation, as shown in Fig.4. So this cavity can work like usual SIW cavity. The resonant frequency is found to be lower about 3% than that of usual solid cavity at 400GHz. And the estimated Q_0 is about 58.



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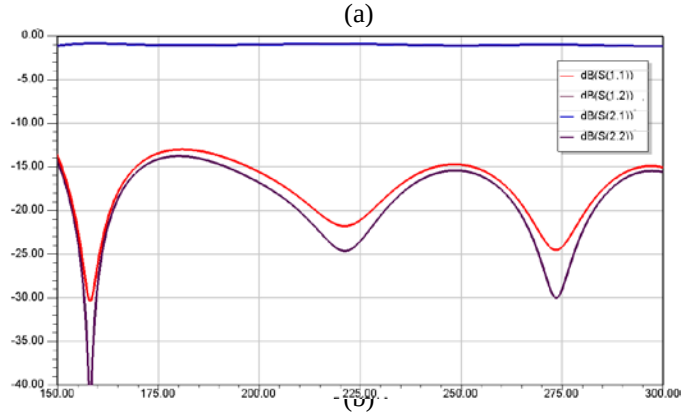
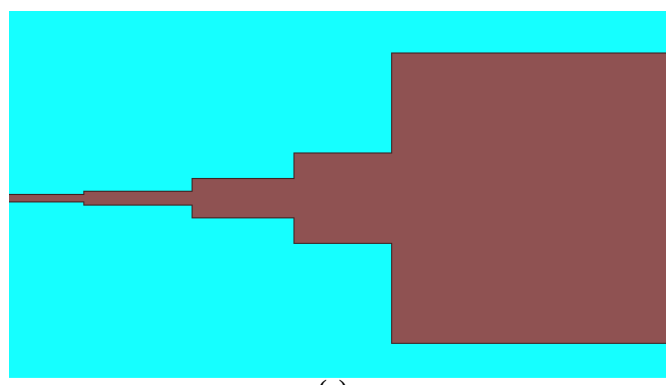


(b)

Fig. 2 (a) Triangular transition from microstrip to SIW with length 1.6mm (b) simulated parameters.



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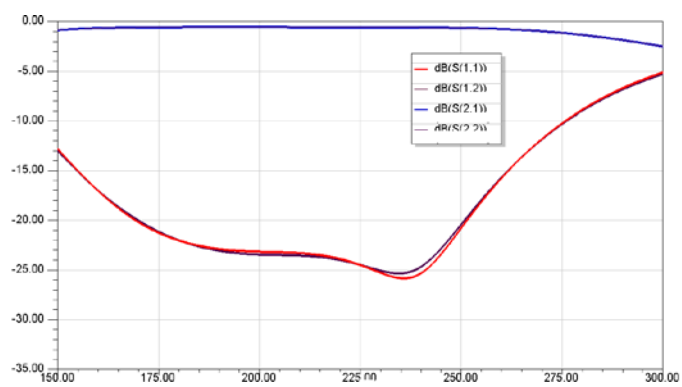
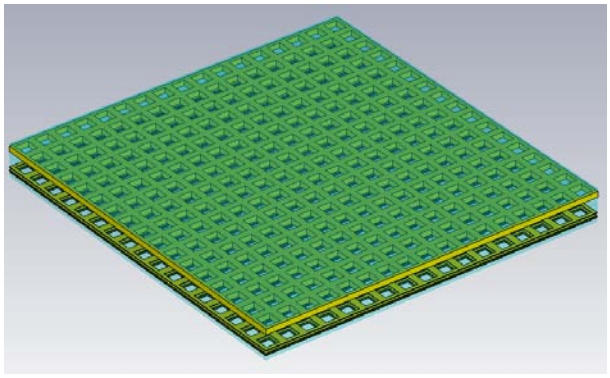


(b)

Fig. 3 (a) 3-sections impedance transformer from microstrip to SIW with length 0.603mm and (b) simulated parameters.



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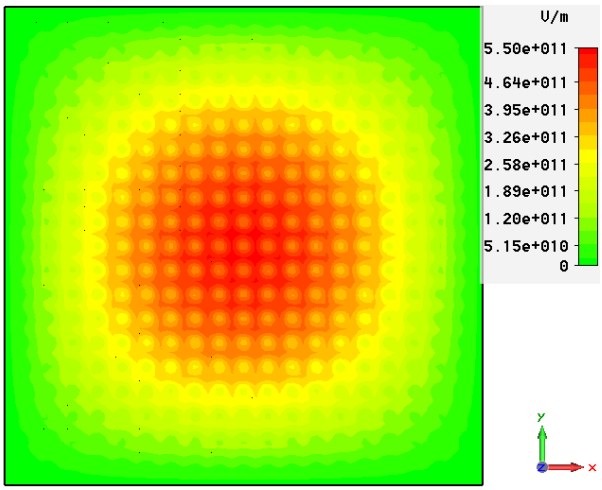


(b)

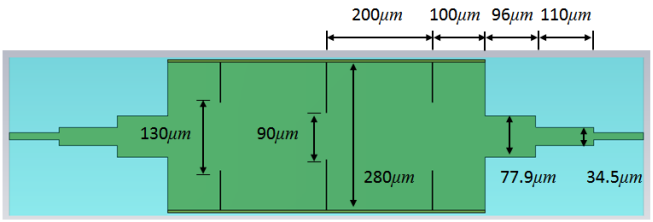
Fig.4 (a)Cavity model based on IBM 130-nm CMOS technology and (b) electric field of TE_{101} mode

D. *Filter on Chip*

According the estimation, the cavity is suit for design filter with a fractional bandwidth great than 3%. Filter design method is according to the traditional SIW filter design [3][4]. A filter with 2 cavities and its simulated results are shown in the fig.5. The -3dB bandwidth is about 37GHz or 9% FBW. Insertion loss is about 1.9dB. Real loss may be great than this value because the simulation neglects some details of structure to simplify the simulation process. The attenuation in stop band is weak. That is common problem of SIW filter with co-line layout but the performance can be improved just by set different layout of cavities [5].

III. Measurement

The filter has been fabricated but is still under testing, so the measured results will be provided in the presentation.



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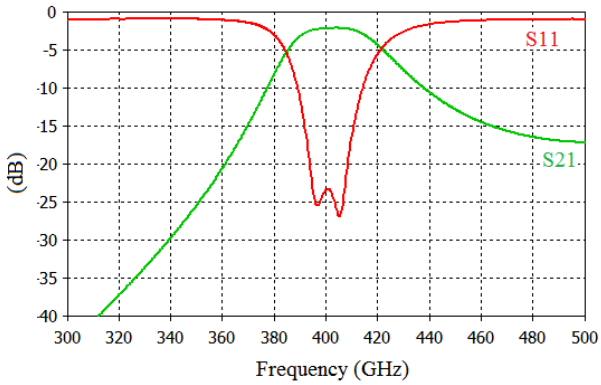

(b)

Fig.5 Filter model(a) and the simulated results(b)

Acknowledgment

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References

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