Development of a waveguide integrated sub-millimetre wave spatially power combined HBV multiplier

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***Abstract*—The development of a sub-millimetre wave, spatially power combined, quasi optical HBV multiplier is presented. Emphasis is placed on key concepts of spatial power combining of frequency multipliers, as well as design challenges. The current state of the design as well as the final goal is further discussed.**

I. Introduction

DURING the past decades considerable effort has been spent on increasing the output power and efficiency of sub-millimetre wave sources.

While sufficient power for single receiver LO drive is available in the sub-millimetre wave spectrum, applications such as radar, communication links and large arrays of receivers call for an increasing amount of output power. Quasi-optical power combination has been successfully applied to e.g. amplifiers at millimetre wave frequencies [1]. However the development of such nonlinear multipliers, by harvesting the harmonics of the input frequency, is more challenging and not yet fully explored. Nevertheless promising results have been published both for continuous, with 684 mW CW output power from an HBV tripler array at 93 GHz [2], and pulsed operation with 24 mW for a Schottky doubler array at 1 THz [3].

GaN MMIC amplifiers are another source for high output powers at W-band. Recent single chip amplifiers produce over 800 mW of output, for which power combined solutions generate multi watt levels [4] [5]. The quasi-optical power combined varactor multiplier presented here is intended to serve as a technology demonstrator for future higher frequency versions. In the sub-millimetre wave region the competition mainly consist of single chip multipliers or binary waveguide combination circuits. The maximum output power from solid-state multipliers at 300 GHz is in the order of tens of milliwatts. The aim of this waveguide integrated HBV multiplier array is to exceed 100 mW at WR-3.4 band, the progress of the work will be presented.

II. Design

The general concept of varactor multiplier design is to present properly chosen embedding impedances to the varactor in and output. On the input side a good source match is needed together with a termination for higher harmonics to prevent propagation in the wrong direction. On the output the input frequency needs a god termination while the desired harmonic must be allowed to propagate. When using the spatial power combination scheme the in- and output filters can be realised by frequency selective surfaces, FSS, in combination with dielectric supports and impedance tuning slabs. The varactors are then embedded in an antenna array designed for good coupling to both the input and output mode. A schematic illustration of the multiplier configuration is shown in Figure 1. One of the motivations for the project is to test to what extent modern computational electromagnetics can be used to optimise the design of spatially power combined varactors. Some parts of the design which aims at a tripler from the WR-10 to WR-3.4 waveguide band are further discussed below.

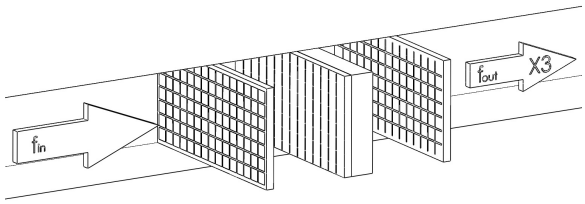

Fig. 1. Conceptual layout of frequency multiplier with half of the waveguide removed, consisting of input- and output filters and matching. The antenna array with varactors is placed in the centre.

A. Filter design

The input filter is a capacitive mesh frequency selective surface, FSS, mounted perpendicular to the propagation direction in the waveguide. The capacitive mesh, acting as a shunt suceptance, forms the input low pass filter. Similarly on the output an inductive strip filter will be used to reflect the fundamental input frequency and pass the third harmonic. One possibility to add electronic tunability to the design is to use varactor loaded FSS filters, the possibilities with that approach has not yet been fully investigated.

B. Array optimisation

The current approach is to first find the gap impedance of the antennas in the array by finite element simulations inside a waveguide. The model used consists of the whole array where the dipoles are approximated as thin wires to save computation time. One problem with embedding an array in a waveguide

structure is the uneven field distribution. Contrary to a free space quasi-optical array where the uniformity of an impinging TEM wave is better than in a TE_{10} waveguide, where the field varies as half a cosine across the extent of the array. The uneven excitation created in a uniform array causes the devices in the centre of the array to saturate long before the other parts of the array reach optimal efficiency. A common behaviour of the efficiency of a HBV tripler as a function of input power can be found in [6].

To mitigate this field non-uniformity and boost the performance for power amplifier grids, the use of a photonic crystal waveguide wall to has been demonstrated [7]. No reports of the use of such structures in multipliers have been found but it is a promising concept. Optimising the diode impedance at the different sites in the array is another way to improve the multiplier performance. By doing so the current distribution in the dipole arms can be made more even and thus the power distribution between the diodes will be improved.

C. Thermal management

Thermal management is an important part of the design in single chip multipliers as well as in arrays and while the thermal effects are investigated in detail for single chip designs little can be found for large varactor arrays. Important considerations to keep in mind is that the power handling and array device density can be limited both by bulk thermal transport problems as well as thermal transport within the diode mesas. Since the bulk thermal conductivity in the InP varactor substrate is poor a heat spreader may be required to heat sink the whole substrate to the mounting waveguide. The heat spreader also adds mechanical support to the brittle InP substrate. Further design considerations are what type of heat-sink that is suitable, some candidates are diamond, SiC and AlN.

III. Conclusion

This presentation presents the current state of development of a multiplier using quasi-optical power combination as an efficient way to overcome the power handling limitations of a single varactor chip. The multiplier is intended to be a stepping-stone in the development of similar devices at higher frequencies.

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