W-band Power Amplifier in 65-nm CMOS

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Abstract- **A W-band power amplifier implemented in an industrial 65-nm CMOS process taking into account reliability issues at high output power level is presented in this paper. On-chip power combining is utilized to achieve high output power with a low supply voltage. The power amplifier has a single-ended input and a balanced output suitable for differential antenna feed. The measured single-ended output power is +11.5-dBm which results in +14.5-dBm differentially. The amplifier is ESD-protected and its silicon area is 0.42 mm^2 only.**

I. Introduction

Several applications utilize the millimeter-wave frequency range (30-300 GHz) since it provides unique characteristics for radio systems [1]. Wide bandwidths are available for telecommunication and commercial local area networks providing gigabit per second data rates. Radar- and imaging systems also benefit from high operating frequency as the resolution increases with frequency. Many of these applications require high level of integration, low cost, and high performance integrated circuits – properties that the rapidly scaled CMOS technology can offer. Scaling the channel length has improved the speed of the transistors significantly, thus enabling mm-wave operation. However, there still are several challenges left for the IC-designer, when designing circuits at these frequencies. The semi-conductive silicon substrate increases the losses of the passives and the voltage swings are limited by the low breakdown voltage of the silicon MOSFET.

The high voltage- and current swings of the power amplifiers (PAs) can have a negative effect on reliability. To guarantee reliable operation, the drain-source voltage swing should not exceed the nominal supply voltage by more than 10%. This is easily violated in a traditional class-A common-source amplifier (CS), where the voltage swings can be twice the supply. The PA presented in this work utilizes a common-gate (CG) transistor in cascode configuration to share the supply voltage with the CS-stage. This guarantees that the voltage swings remain within the safety limits even under extreme operation conditions.

This paper presents a compact sized, ESD-protected, W-band (75-110 GHz) CMOS PA implemented in a 65-nm low power (LP) CMOS process taking into account the industrial requirements. The PA has four parallel unit amplifiers with single-ended input and balanced output. Section II describes the amplifier design and the passive components used in the PA. Measurements results are shown in section III.

II. Amplifier Design

Since reliability issues limit the maximum voltage swings in the transistor, current must be increased to obtain higher output power. The size of the power device is also restricted at mm-wave frequencies as the device- and contact parasitics start to limit the performance of MOSFETs. One solution to obtain higher current swings is to use several unit amplifiers and on-chip power combiners. Fig. 1 shows the simplified schematic of the PA. It consists of four unit PAs, which each utilize three balanced cascode stages. Microstrip-line based current-mode power dividers and combiners are used at the input and at the output. Matching and single-ended to differential conversion is performed with integrated transformers.

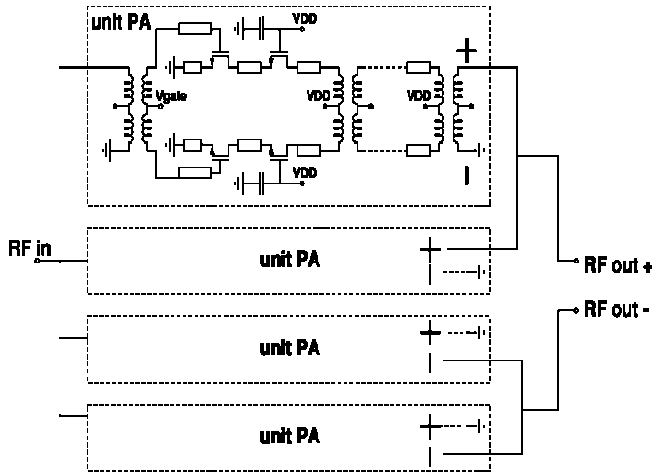

Fig. 1. Simplified schematic of the PA.

A. Active device selection

The unit amplifiers are based on cascode topology for higher gain, isolation, and stability. Moreover, the supply voltage is now shared between the stacked common-source and common-gate transistors, reducing the voltage stress and therefore ensuring reliability. This guarantees that the drain-source voltage of each device stays below the maximum rating ($V_{DS\text{-}RMS}$~$1.1xV_{DD\text{-}nom.}$), even under large signal operation.

The unit PAs consists of three stages, which utilize differential cascode pairs. Each transistor is sized at minimum gate length (60 nm) and consists of four parallel devices that have 22, 24, and 28 fingers in the CS transistors, and 26, 28, and 32 fingers in the CG transistors in stages 1, 2, and 3, respectively. The unitary finger width is set to 0.9 µm for maximum f_{max}.

B. Transformers

The utilized CMOS process provides two thick copper layers that are suitable for implementing a stacked conductor transformer. This type of vertical structure yields tight coupling between the primary and secondary coils as well as compact size. The required inductance values are small at mm-wave frequencies and, typically, a single-turn transformer is sufficient.

Transformers are used mainly for matching purposes and single-ended to differential conversion, however, they are also suitable for DC-biasing through the center taps and DC-decoupling between amplifier stages. This removes the need for decoupling capacitors, which typically have high loss and modeling uncertainties at mm-wave frequencies. The input and output of the PA are inherently ESD-protected, as the winding connected to the pad is grounded at the other end and it therefore provides a low resistance path for ESD-currents.

Performance is validated with EM-simulations, which can also capture parasitic capacitances that result from dummy metal fillings. The inductance of the windings is controlled mainly by the inner diameter that ranges from 15 to 30 µm. The minimum trace width is set according to the electromigration design rules for DC-current, since the biasing current of the amplifier stages flows through the transformer windings. The diameter and trace width of the primary and secondary winding can be varied to provide desired impedances for the input and output matching networks of the transistors. This is especially useful in a PA, in which the driver stages are often designed to be smaller than the power stage to enhance the power added efficiency (PAE).

C. Power combiners and interconnects

Interconnects must be accurately modeled at mm-wave frequencies and, especially, the substrate effects should be considered carefully. The use of microstrip line topology is beneficial since it allows complete substrate shielding and, thus, fast and accurate EM-simulation. Top metals are used for the signal line and the ground plane is at metal 2-layer. The trace width varies from 4 µm to 8 µm and, again, the minimum trace width is set by the electromigration design rules for DC-current. When matching is performed with transformers, the inductive quality factor of a transmission line is not the main design parameter. This is in contrast to transmission line-based matching schemes, where a high line inductance is desired.

The on-chip power division and power combining can be implemented with a simple microstrip divider tree. This approach does not provide as high isolation between the output ports as the Wilkinson-topology, but its implementation is straightforward and it consumes less silicon area. Additionally, the transformers provide inherent power division, when used as a single-ended to differential converter. Fig. 2 shows a power division method using microstrip divider and transformers.

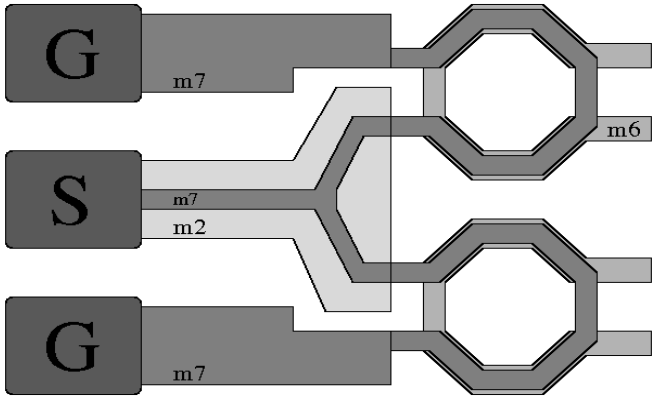

Fig. 2. Simplified layout of a microstrip divider and transformers that perform matching and single-ended to differential conversion.

III. Measurement Results

The measurements were performed with 1.2 V supply in single-ended configuration since balanced RF-probes were not available at this high frequency. The measured and simulated S-parameters are in good agreement with each other and the results are shown in Figs. 3 and 4. The gain is 10 dB at 90 GHz and the 3-dB bandwidth spans over 20 GHz.

The PA is unconditionally stable at the operation frequency, however, some low-frequency oscillations were observed during the measurements. It is expected that the oscillations result from the DC-biasing cables and that they can be attenuated by bonding the chip to a printed circuit board that allows placement of external capacitors and resistors close to the DC-pads. In simulations oscillations were not observed, as each stage was separately designed to be unconditionally stable over the entire frequency range.

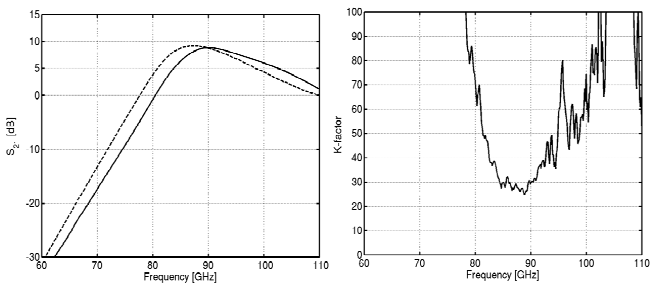

Fig. 3. Measured (▬) and simulated (- - -) S_{21}-parameter and measured stability factor of the PA with a 1.2 V supply.

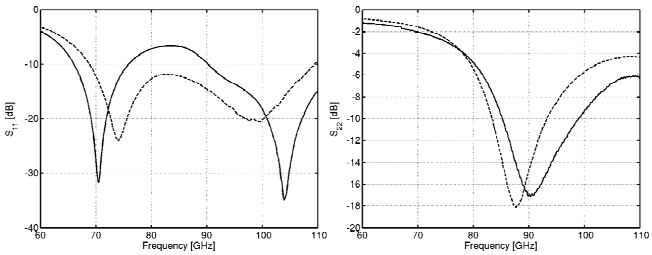

Fig. 4. Measured (▬) and simulated (- - -) input and output reflection coefficients with a 1.2 V supply

The output power was measured from both output ports in single-ended configuration since balanced RF probes, which can operate at the desired frequency, were not available. The measured maximum output power was +11.5 dBm, which should give +14.5 dBm of differential output power. Fig. 5 shows the AM/AM-characteristics of the PA and Fig. 6 shows the maximum differential output power over frequency. The latter was obtained by adding 3 dB to the single-ended result.

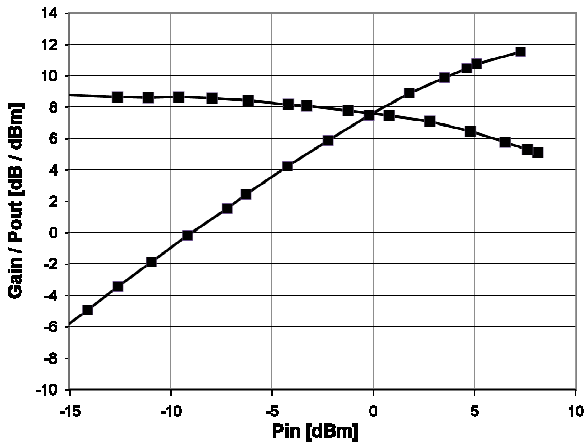

Fig. 5. Measured (single-ended) gain and output power of the PA with 1.2 V supply.

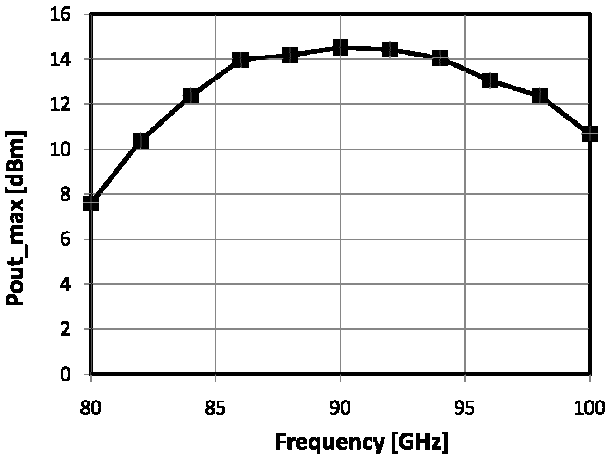

Fig.6. Measured differential maximum output power of the PA with 1.2 V supply.

Table I collects the measured performance characteristics and compares them to recently published CMOS amplifiers operating at W-band. The presented performance is achieved, while taking into account the industrial requirements for reliability and manufacturability. Miniature chip-size is obtained with extensive use of on-chip transformers. The chip micrograph is shown in Fig. 7, from which the four unit PAs can easily be identified.

TABLE I
PUBLISHED W-BAND CMOS PAS

	This Work	[2]	[3]	[4]	[5]
Technology	65nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS
Topology	Cascode 4-way	CS	Cascode	Cascode	CS
Supply [V]	1.2	1.2	3	3	1
Freq. [GHz]	90	100	94	80	80
P_{sat} [dBm]	+14.5	+10	+12	+11.8	+10.3
OCP_{1dB} [dBm]	8	6	8	9.3	7.5
PAE [%]	4	7.3	5.2	6	4.5
Gain [dB]	10	13	15	18	12.2
3dB BW [GHz]	20	21	17	15	19[b]
Area [mm²]	0.42[a]	0.33	0.4	0.656	0.56
P_{sat}/area [mW/mm^2]	67	30	40	23	19

[a] Active area 0.17mm² [b] 1dB bandwidth

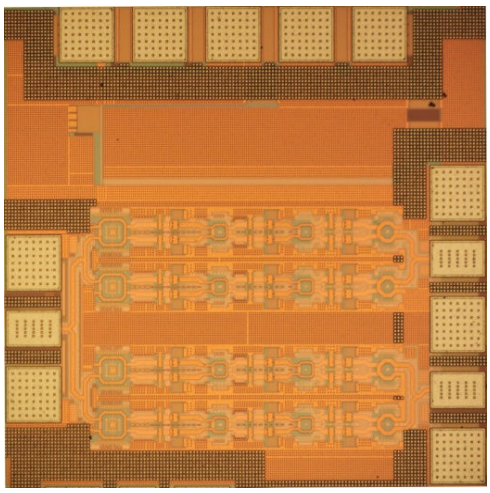

Fig 7. Chip micrograph of the power amplifier. The size, including RF- and DC-pads, is 0.42 mm^2.

ACKNOWLEDGMENT

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