A Novel 332 GHz Planar Integrated Frequency Doubler

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Abstract- **The design and development of a novel planar integrated frequency doubler operating at 332 GHz using Rutherford Appleton Laboratory varactor Schottky diodes is presented. Preliminary measurement results of the device show a peak efficiency of ~14% at 332 GHz and a 3 dB bandwidth of ~7%. Measured results are in close agreement with the modelled performance. An improvement in the doubler performance, especially at lower frequencies, is expected as the device has been driven with lower than optimum pump powers so far.**

Keywords: Frequency doublers, millimetre waves, radiometry, GaAs Schottky diodes

I. INTRODUCTION

In the past, terahertz technology has mainly been driven by the requirements of astronomy and atmospheric remote sensing. Recently, it has expanded into new avenues such as security imaging, surveillance, DNA/tissue mapping and communication [1]. There are clear advantages for using terahertz frequencies for these applications and the demand for reliable and robust high frequency sources exhibiting high output power, efficiency and large operating bandwidth is growing significantly.

Sensitive high resolution spectral measurements in, for example astronomy, earth observation and atmospheric science, necessitate the use of heterodyne receivers. Frequency multipliers have been mainly used to generate local oscillator (LO) power for these receivers [2]. These multipliers use either Schottky [3] or Heterostructure Barrier [4] varactor diodes. Multipliers operating at higher harmonic orders or cascaded lower harmonic multipliers are required to generate the necessary power at near terahertz frequencies. The other potential technologies for generating power at THz frequencies include quantum cascade lasers or photonic down conversions by mixing optical laser beams in a high speed photodiode [5]. However, quantum cascade lasers have not been demonstrated for frequencies below 1 THz and in photomixing efficiency drops off rapidly with frequency such that it is not likely to deliver sufficient LO power for operating Schottky mixers above 200 GHz. It is anticipated that multiplier circuits will remain as the main technology used for receiver local oscillator power generation for the foreseeable future.

The multiplying efficiency and power handling capability of Schottky varactor diodes can be enhanced by removing GaAs from underneath the diodes and transferring the chip onto a higher thermal conductivity, electrically low loss, substrate [6,7]. The power conversion efficiency of Schottky multipliers increases with the applied input power, for example a doubler operating at 160 GHz with 100 mW input power gives efficiency of ~35% [8].

We have developed sources operating at the same frequency with 30% efficiency and 15% bandwidth (BW) from 50 mW input power using discrete varactor diodes produced at the Rutherford Appleton Laboratory (RAL) [9]. High efficiency operation for these multipliers at comparatively low input power is achieved by transferring the varactors from GaAs to low loss quartz substrates.

Local Oscillator for 664 GHz channel proposed for future Earth Observation missions

In this paper, we present the results obtained for a frequency doubler, designed to deliver power at 332 GHz using RAL varactor technology. The doubler satisfies the LO output frequency requirement of the 664 GHz receiver channel proposed on future atmospheric remote sensing missions to monitor ice clouds in the atmosphere, e.g. the CIWSIR Earth Explorer mission [10] the MetOp second generation series of satellites [11]. One of the preparatory activities to establish the feasibility of these missions is the build and deploy a sub-millimetre wave airborne demonstrator (ISMAR) for both ice cloud and precipitation observations [12]. ISMAR currently has one operational channel at 325 GHz with provision to add high frequency channels including 664 GHz as the technology becomes available.

For the design presented here we adopt an integrated approach, which has allowed us to design highly functional multiplier chips with micron dimensions and accuracies. The integrated chip is transferred on to aluminium nitride substrate which allows the easy dissipation of heat generated in the anodes. The availability of advanced electromagnetic simulation tools and a careful design approach has enabled us to make design predictions for these high frequency circuits with reasonably good accuracy.

II. ELECTROMAGNETIC MODELLING AND PREDICTIONS

Ansys HFSS and Agilent ADS are used to model the varactor and associated circuitry of the doubler block. Figure 1 shows the HFSS model of the integrated doubler and an expanded view of the diode array. The circuit configuration consists of four varactor diodes arranged in anti-series configuration in the input waveguide. This balanced design generates only the even mode harmonics of the input frequency.

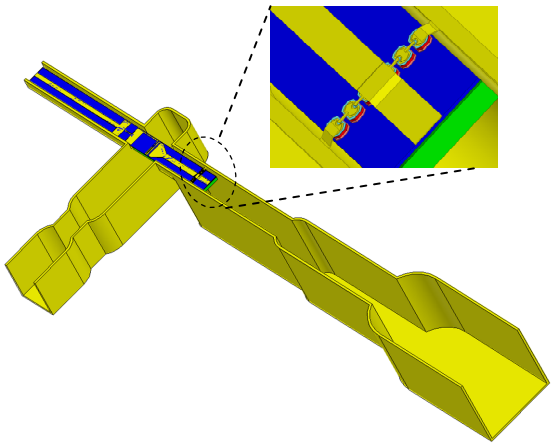


Figure 1 HFSS model of the 332 GHz doubler

Generated harmonic power propagates in a microstrip mode and is coupled into the output waveguide by a bow-tie probe. DC bias can be applied thorough a stripline RF choke connected to the other side of the probe. In principle, generated second harmonic power could be lost by propagation in the input waveguide in an unbalanced TM_{11} mode. This is prevented by reducing the height of the input waveguide at the location of the MMIC. Furthermore, the microstrip channel height just after the input waveguide is reduced to prevent the propagation of the input frequency further; this enables isolation between the input and output frequencies without using filters.

The optimum embedding impedances are calculated using Agilent ADS from the non-linear simulations optimising the single varactor diode in the frequency band 320 to 340 GHz at the expected drive level, in this case an input pump power of 10 mW. The optimum and calculated embedding impedances for selected frequencies in the band is presented in Table 1 below.

TABLE I
Optimum and calculated embedding impedances for a 332 GHz balanced doubler

Output Frequency (GHz)	Z_{in} (Ohm)		Z_{out} (Ohm)	
	Optimum	HFSS	Optimum	HFSS
320	19+j112	11+j105	12+j56	7+j50
330	19+j105	12+j100	12+j52	8+j55
340	18+j107	7+j105	11++j53	10+j70

It can be noted from the table that the optimum embedding impedances changes slowly with frequency and this allows larger bandwidth without using mechanical tuners.

A bow-tie T-line transition [13] is used to couple energy from the stripline to a full height output waveguide and the reflection coefficient for the transition across the band is shown in Figure 2.

The graph in Figure 3 shows the calculated input reflection coefficient verses output frequency for different input power levels. The predicted results shows that the doubler gives a reflection coefficient better than 20 dB at the design frequency 332 GHz for 40 mW input power (10 mW/anode), the power for which the design is optimised.

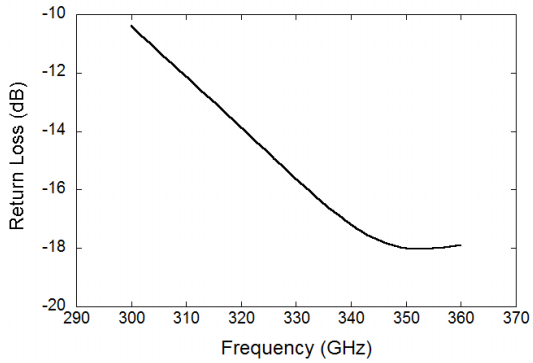


Figure 2 Return Loss for the Bow-tie T-line transition

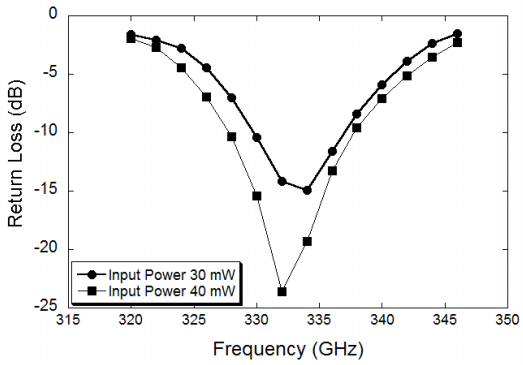


Figure 3 Predicted input reflection coefficient versus output frequency for different input power

Figure 4 shows the output power and efficiency predicted for the design for series anode resistance of 4 Ω and optimised pump power 40 mW. The simulated responses for the design for anode resistance 6 and 7 Ω and input pump powers of 20 and 30 mW are shown in Figure 5. The diode resistance and the drive power for the curves shown in figure 5 are selected based on the typical measured series resistances and the available drive power for testing.

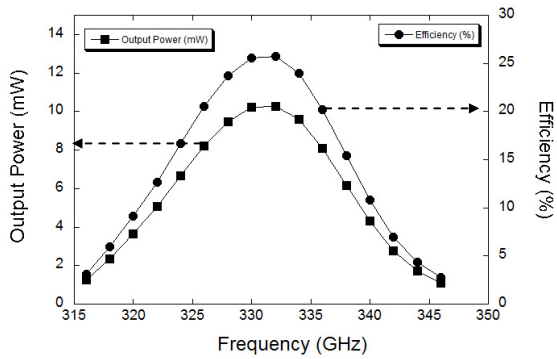


Figure 4 Predicted performance of the doubler for the optimum pump power of 40 mW and expected diode series resistance of 4 Ω

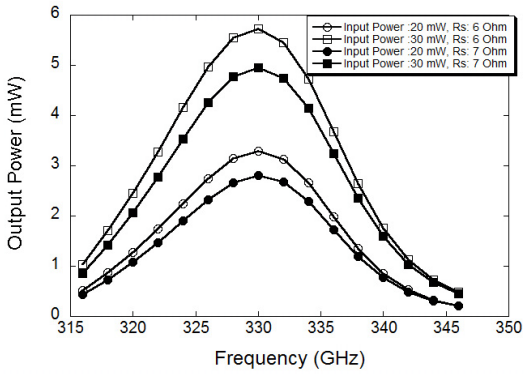
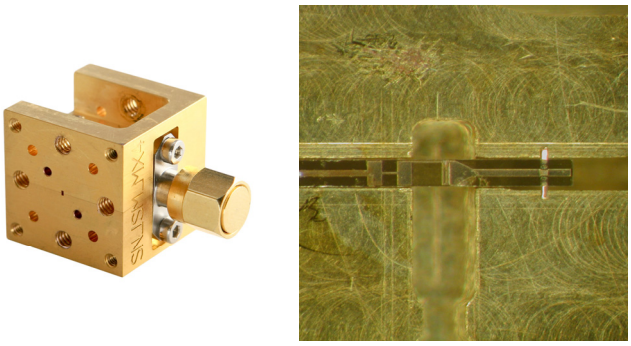


Figure 5 Predicted performance of the doubler corresponding to the measured series resistance and available drive power for testing

III. Design and Construction

The 332 GHz frequency doubler features an integrated MMIC chip consisting of Schottky varactor diodes and the associated matching circuitry fabricated at the RAL Schottky diode facility. The waveguide doubler block and the photograph showing the circuit mounted inside the split block is shown in Figure 6. The chip is initially fabricated on a gallium arsenide substrate and is subsequently transferred on to aluminium nitride as the latter exhibits low loss and high thermal conductivity at millimetre and sub millimetre wavelengths [6]. The integrated chip consists of four Schottky varactor diodes arranged in anti-series configuration in the input waveguide, a centre stripline for propagating the input frequency as TEM mode, a probe for coupling the power to an output waveguide and an RF filter for the dc biasing network [14] .



(a) (b)

Figure 6 Photograph of a 332 GHz doubler (a) block (b) inside view showing varactor diodes and associated circuitry

At high frequencies it is necessary to reduce the anode diameter to reduce the net capacitance, and to increase the epitaxial layer doping to delay the onset of velocity saturation. An epitaxial layer doping density of 2 x 10^{17} cm^{-3} and a buffer layer thickness of 6 µm is chosen for the current design.

Figure 7 shows the scanning electron micrographs of the integrated varactor diode filter assembly inside a split block waveguide. The overall chip dimensions are 1.2 mm x 0.16 mm x 0.040 mm and the varactor anode diameter is 3.6 µm. The calculated resistance of a single varactor diode used in this design is 2.6 Ω, which includes spreading resistance, epitaxial layer resistance, and buffer layer resistance [15, 16]. The grounding to the varactor diode branch is provided using beam leads: see Figure 7. The requirements of impedance matching and need to control mode generation means the input waveguide height must be reduced at the position of the diode array. For this design, quarter height input waveguide is used, 0.2 mm high. The general design approach is to place the diodes closer to the waveguide walls, or use substrates of high thermal conductivity, to enable adequate heat dissipation. The position of the diodes inside the waveguide decides the coupling to external circuitry and the distance between the anodes is optimised to achieve almost equal coupling from the two diode branches to the circuit.

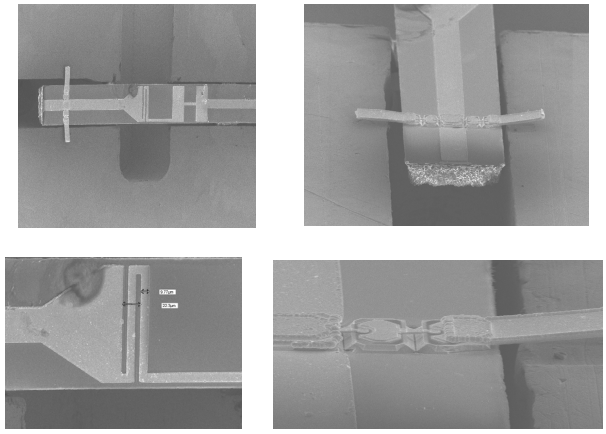


Figure 7 Electron micrographs of the beam lead chip in position in the waveguide block.

IV. Measurement Setup

The doubler was tested at input frequencies between 160 to 170 GHz. The input drive power for the doubler comprised of a Carlstrom Gunn oscillator for W band power generation (60-80 mW) followed by a VDI doubler [VDI D162], which generated between 12 and 33 mW for output frequencies between 300 to 345 GHz. The measurement setup is calibrated initially by measuring the output power from the doubler using an Eriksson power meter and a WR5-WR10 waveguide transition as shown in Figure 8. The output power and efficiency of the RAL doubler under test is measured using the power meter and a WR3-WR10 transition. Corrections to measured powers are made appropriately for losses in the transitions.

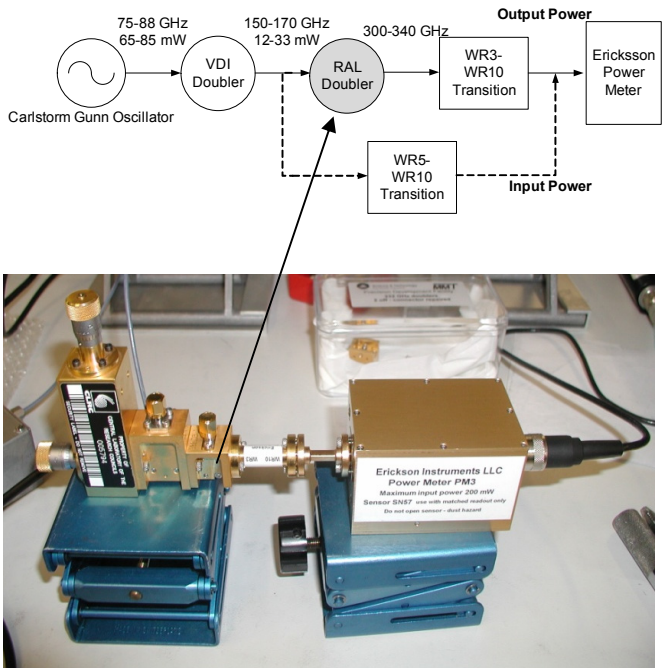
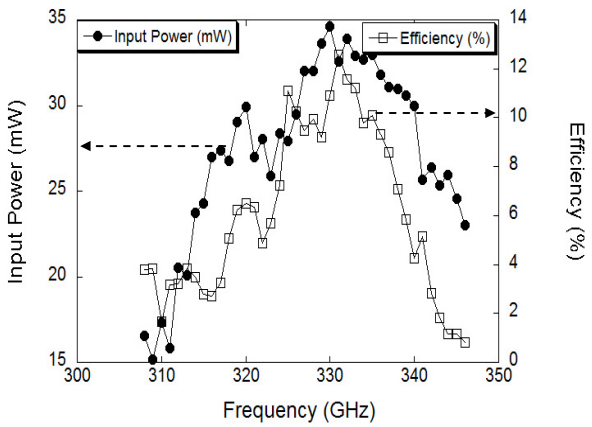


Figure 8 Measurement setup for RAL doubler performance measurement

V. Experimental Results

The measurement results are presented for a doubler using two different MMICs mounted inside the same waveguide block, and those two MMICs are selected from the same batch obtained from a single wafer process run. Figure 9 shows the measured efficiency plotted for the maximum available input power for both circuits. Circuits 1 and 2 show almost similar performance: circuit 1 exhibits a peak efficiency of 12.8 % at 332 GHz and circuit 2 yields 13.5 % at 328 GHz. There is a slight variation in the input power profiles due to the variation in VDI doubler bias between two measurements.



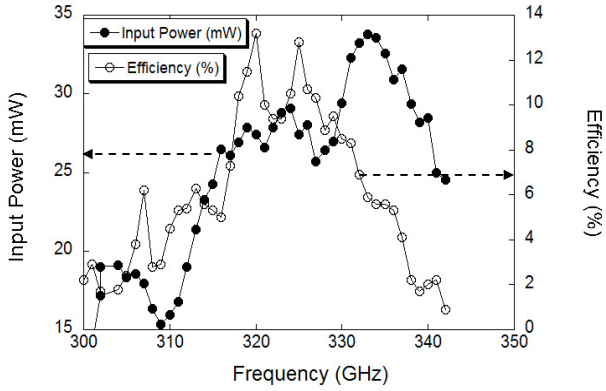


Figure 9 Input power and the efficiency measured for the novel 325 GHz doubler using two different varactor MMICs from the same wafer.

The curve shown in Figure 10 is the output power measured for circuit 1 for the input power given in the top plot of Figure 9. A diode resistance of 6 to 7 Ω is measured for a single anode in these chips and the input power applied varied between 12 to 33 mW for different input frequencies. The curve shows that the measured output power varies between 0.2 and 4 mW in the frequency band 315-345 GHz. The graph also shows the predicted performance for a constant 30 mW input power and 7 Ω diode series resistance. There is close agreement between the measured and modelled performance.

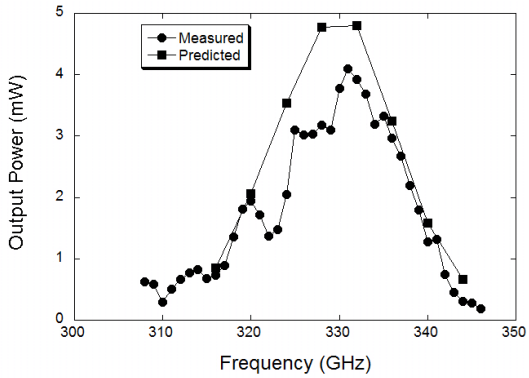


Figure 10 Output power verses frequency measured for the 332 GHz doubler for circuit 1. The predicted performance plotted is for 30 mW input power and 7 Ω diode series resistance

In the model, the doubler circuit has been optimised for a pump power of 40 mW throughout the frequency band. However, the doubler is tested at a drive power at much lower level than the optimum due to the unavailability of enough pump power for testing. The doubler is significantly under pumped, especially at frequencies up to 330 GHz and it is expected that the efficiency will improve with an increased drive level. At 332 GHz the output power is measured sweeping the input pump power and the efficiency calculated: Figure 11. The efficiency increases linearly with frequency, indicating that doubler is not operating at a saturated drive level. Therefore, an improvement in efficiency can be expected with increase in drive power, even at the higher edge of the band.

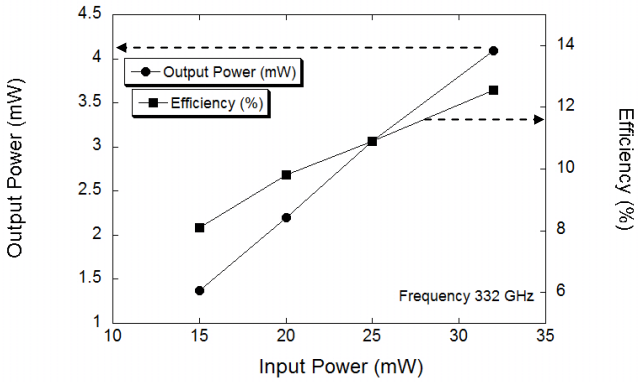


Figure 11 Output power and efficiency plotted vs. input power at 332 GHz.

Bias is provided via an external dc supply. The graph of dc bias voltage and current versus output frequency is shown in Figure 12. The bias is optimized at each frequency to deliver maximum power at the second harmonic. The anti-series arrangement of the doubler has two anodes in each branch, so that the voltage applied to each anode is one half of that shown in the graph, and similarly the current per pair is half the indicated amount. The current drops towards zero at 332 GHz, the point where the peak efficiency is observed.

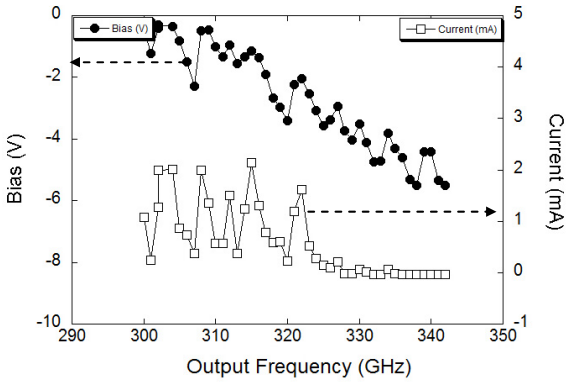


Figure 12 Measured dc current and bias voltage versus output frequency for the doubler circuit.

VI. Discussion

The measured performance agree reasonably closely to the predicted performance as shown in Figure 10. Input power and anode resistance applied for generating simulation curve in the comparison plot are the measured anode resistance and input power applied to the real circuit.

Swept input power measurements for the doubler indicates that the efficiency and bandwidth of the circuit will improve by increasing the drive power throughout the band. The measured diode resistance is quite high, ~ 6/7 Ω, compared to the calculated value of 2.6 Ω. It is anticipated that current iterative wafer runs will deliver devices with a lower series resistance. From the efficiency curve plotted in Figure 13, a peak efficiency above 20% could be achieved by using the same circuits with a diode of 4 Ω resistance .

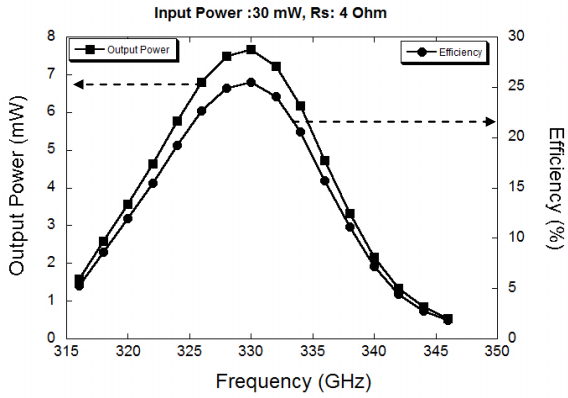


Figure 13 The predicted efficiency for a circuit using diodes of series resistance 4 ohms

Alternatively, Figure 14 shows the predicted performance for the doubler block using circuits with the same resistance as the measured ones but with more input drive power.

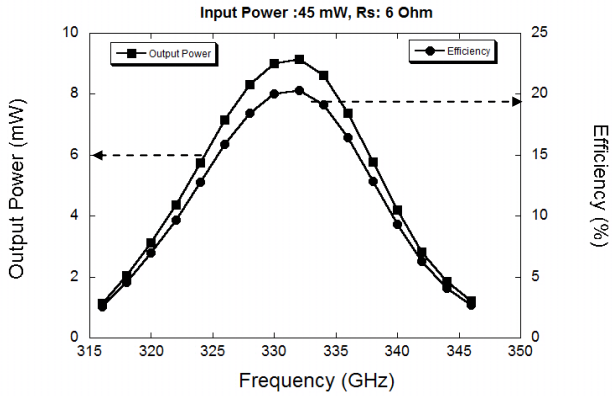


Figure 14 Predicted efficiency for the as-built doubler circuit for a 45mW drive power

Figure 13 and 14, both indicate that an efficiency above 20% could be achieved by using the same doubler circuit with lower diode series resistances or by using higher drive power with the current, as-built, circuit.

VII. Conclusions

A novel 332 GHz integrated doubler based on transferred substrate technology has been demonstrated. The doubler gives a peak efficiency of 13.6% at the design frequency 332 GHz. The 3 dB bandwidth measured for the design is ~7%. Predicted and measured performances are in good agreement. It has been established by simulation and measurements that the performance of the existing doubler could be significantly improved by increasing the input drive power. It has also been shown that the MMIC circuit will perform better if lower series resistance diodes can be produced. The creation of circuits with lower series resistance is underway.

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