A Broadband Low-Noise D-Band Amplifier Module in 35 nm mHEMT Technology

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***Abstract*- This paper presents a broadband low-noise amplifier MMIC in D-band (110-170 GHz), manufactured with the Fraunhofer IAF 35 nm metamorphic high electron mobility transistor (mHEMT) technology. The chip size is 1.0 × 2.0 mm^2 and it was packaged into a split-block module with integrated DC-control. Small-signal gain, noise figure and linearity were measured and the reported results demonstrate state of the art values of over 20 dB gain in a 50 GHz bandwidth, noise figure of below 4 dB and a 1-dB compression point of -22 dBm input power.**

I. Introduction

Low-noise amplifiers (LNAs) are typically the crucial first stage in receivers for data-links, spectroscopy or millimeter-wave imaging. Since the noise figure (NF) of the LNA adds directly to the system NF according to Friis formula, its low-noise performance is essential for a well-engineered receiver of any kind [1]. Simultaneously, LNAs need to provide sufficient small-signal gain to minimize the impact of noise contributions of the subsequent stages. Two LNAs satisfying these basic specifications were previously reported in [2].

The increasing demand of consistently increasing data-rates in high-speed communication and of sensitivity and resolution in imaging systems requires furthermore very broadband designs. The presented LNA covers the entire D-band, providing high absolute bandwidth and including the atmospheric window around 140 GHz which is significant for wireless communication and imaging. The coverage of the 118 GHz oxygen line makes this LNA also applicable for spectroscopy.

II. Technology

For high frequency and ultra low noise applications the mHEMT based on InGaAs/InAlAs heterostructures with high In-content in the electron transport channel is the most appropriate device. These heterostructures can either be grown directly on InP substrates or by using a metamorphic buffer to adapt the lattice constant on GaAs wafers. The latter option allows to process highly integrated ultra low noise circuits on cost-efficient GaAs wafers. Fraunhofer IAF features a mHEMT technology with different gate lengths. The mHEMT layers are grown on 4″ semi-insulating GaAs wafers by molecular beam epitaxy (MBE). To suppress parasitic substrate modes the technology offers a backside process, where the wafers are thinned down to a final thickness of 50 µm. Subsequently, through-substrate vias with 20 µm contact diameter to the front side are processed by dry etching and finally, the wafer backside is gold plated.

The presented LNA was designed and processed using transistors with 35 nm gate length. This technology exhibits a channel mobility and a channel electron density as high as 9800 cm^2/Vs and 6.1×10^{12} cm^{-2}, respectively. The maximum extrinsic transconductance $g_{m,\,max}$ is 2500 mS/mm and a transit frequency f_T of over 500 GHz was achieved [3].

III. Low-Noise Amplifier Design

The low-noise amplifier has been designed using grounded coplanar waveguide (GCPW) topology. All transistors in the four-stage design are in common source configuration with a gate width of 2 × 15 µm, each. Inductive source degeneration with symmetric source transmission lines was used to increase stability and improve noise behavior [4]. Furthermore, the IAF technology allows to integrate NiCr thin film resistors and metal-insulator-metal (MIM) capacitors for RF-decoupling. Fig. 1 shows the schematic of the LNA. Matching networks consisting of shunt stubs with different line impedances and series capacitors were used to adapt to the input- and output impedances of the transistors. Although no special broadband design techniques were used, the focus of the circuit design was to achieve a broadband gain characteristic rather than ultra low noise performance. The processed microwave monolithic integrated circuit (MMIC) has a die size of 2 × 1 mm^2 as can be seen in Fig. 2.

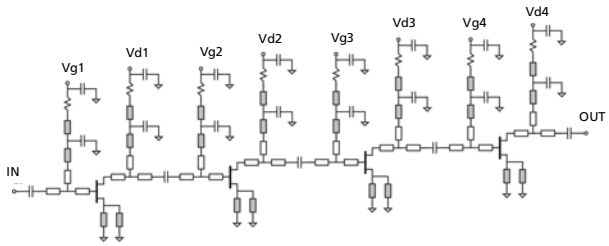

Figure 1. Schematic diagram of the four-stage LNA with symmetric source feedback and the RF-block and DC supply network with on-chip capacitors and resistors.

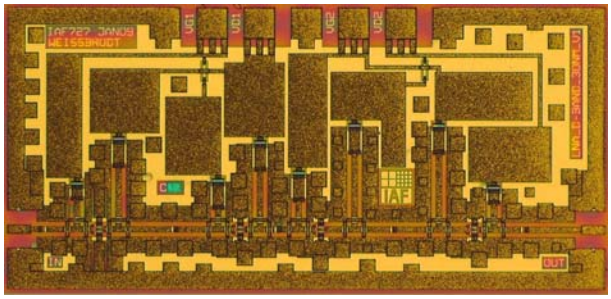

Figure 2. Chip photograph of the processed D-band LNA MMIC (2×1 mm^2) with grounded coplanar waveguide transmission lines and large on-chip capacitors.

IV. Simulations and on-chip measurements

The LNA design was simulated in ADS, using IAFs proprietary libraries, including models of passive and active devices based on extractions from measurements up to 110 GHz. The transistor model features noise parameter prediction and is bias dependant [5].

The simulation results of the S-parameters and the noise figure are shown in Fig. 3 (solid lines) and compared to on-chip S-parameter measurements (dashed lines). The applied gate voltage was -0.1 V and the drain voltage was 0.8 V, yielding a drain current density of 430 mA/mm. This results in a total DC power consumption of 41.3 mW. The simulation shows a very flat gain of around 23 dB over the entire D-band, whereas the measurement result exhibits a slowly decreasing gradient from about 26 dB at 110 GHz to 16 dB at 170 GHz. This inconsistency might be due to the limitation of the modeling data up to 110 GHz. Also, the input and output return losses show some discrepancy between simulation and measurement. However a good matching of below -10 dB was achieved over the bigger part of the D-band.

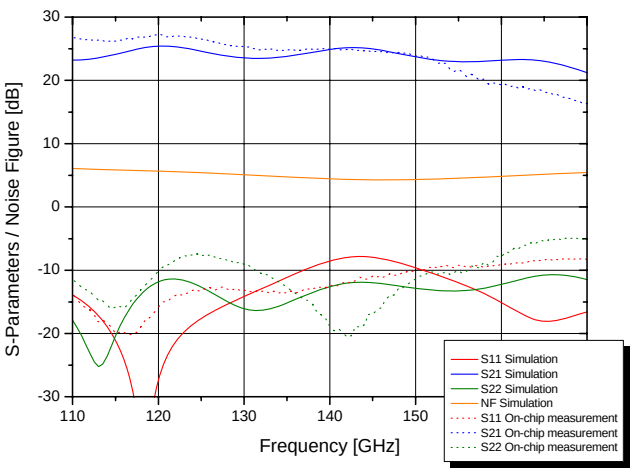

Figure 3. Simulated S-parameters and noise figure (solid lines) and on-chip measured S-parameters (dashed lines) of the D-band LNA MMIC.

V. Packaging and module-measurements

The MMIC was packaged into a waveguide module with an integrated programmable DC-control board. Fig. 4 shows the MMIC mounted into the open split block package. One can see the waveguide transitions as well as the transitions from grounded coplanar to microstrip lines at the signal ports of the LNA. The DC-pads of the MMIC are wire bonded to DC-lines which are connected by electrical feedthrus to the DC-control board on the backside which can be seen in Fig. 5. Note that the chip layout allows the first two transistor stages and the subsequent two stages to have separate DC-supplies. While all four transistors are operated with the same gate voltage in the module, the DC-control board allows to allocate different drain voltages for the first two (drain1) and the subsequent two (drain2) stages. This permits to fine-tune the LNA for optimum gain-to-noise-ratio.

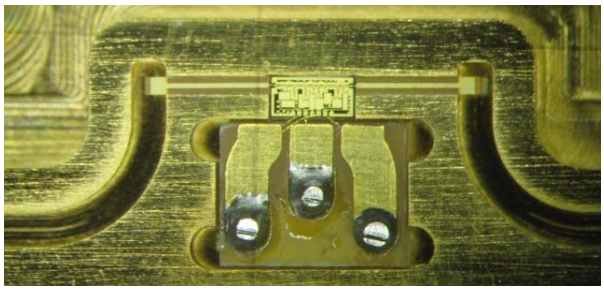

Figure 4. Photograph of LNA MMIC mounted into open split-block package with waveguide transitions and bonded to DC-pads which are connected by electrical feedthrus to the DC-control board on the backside.

For the presented S-Parameter measurements of the module, drain1 was set to 0.8 V and drain2 to 1.0 V, while the gate voltage was set to -0.1 V. The voltage control is performed within the module which itself is only connected to a 5 V voltage supply which can be seen in Fig.5. The result of the measurements is shown in Fig. 6.

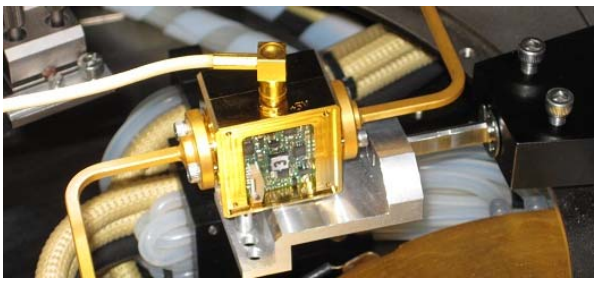

Figure 5. LNA module with integrated DC-control circuitry, connected to a 5 V DC-supply and waveguide measurement setup.

The LNA module exhibits a small-signal gain (S_{21}) of over 20 dB in a frequency range of 50 GHz and covers the entire D-band with a linear gain of more than 15 dB. Input- and output return losses (S_{11} and S_{22}) of the LNA are better

than -5 dB in the entire band. The gradient in gain can be observed again and is identical to the on-chip measurement. Losses due to the packaging and the waveguide transitions are compensated by the modified operating voltages.

Noise figure measurements were performed with a recalibrated noise diode. The setup allowed measurements in the frequency range from 113 to 150 GHz, where the LNA module achieves a state of the art noise figure of below 5 dB and even below 4 dB between 115 and 135 GHz (Fig. 6).

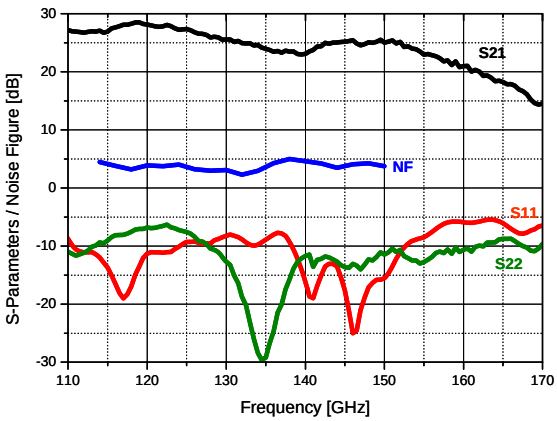

Figure 6. Measured S-parameters and noise figure of the packaged LNA MMIC.

Even though LNAs are not designed to handle high power levels, their compression and intermodulation performances must be adequate to provide enough dynamic range for e.g. imaging applications. Therefore, it is important to know large signal characteristics when dimensioning receiver systems or calculating power budgets. Linearity measurements were performed at the center frequency of 140 GHz. Fig. 7 shows the measured output power and the calculated gain for input power from -25 dBm to -11 dBm. The 1-dB compression point is located at -22 dBm input power, which is a typical value for InGaAs low-noise amplifier circuits.

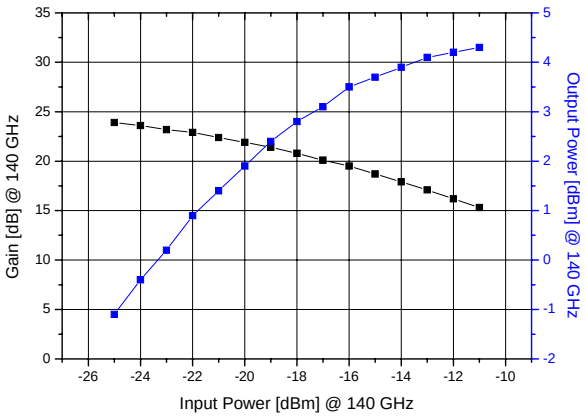

Figure 7. Measured output power and gain of the D-band LNA module.

VI. Conclusions

A broadband low-noise D-band amplifier was designed, simulated and processed with our in-house 35nm mHEMT technology. Simulations and on-chip measurements were compared and the packaging into a split-block module described. The LNA module was then extensively characterized, demonstrating excellent gain and noise performance over a large bandwidth. Compared to other published work on LNAs in various technologies, this work achieves some outstanding figures of merit (FOM). Fig. 8 shows the gain-bandwidth product of several published LNAs at their center frequencies. Since this figure presents the absolute bandwidth, similar FOM as in this work were achieved at higher frequencies.

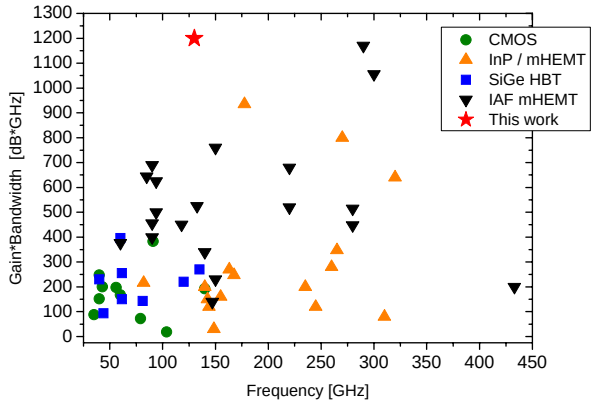

Figure 8. Product of gain and bandwidth of various LNAs as a figure of merit at their center frequency. Several state of the art results are shown, realized in different semiconductor technologies.

Fig. 9 shows the published noise figures of LNAs in several semiconductor technologies. Note that accurate noise figure measurements at these frequencies are challenging and not all published work can present their noise figures. Also, most of the noise figures in Fig. 9 were measured on chip, neglecting the degradation associated with waveguide packaging. As in Fig. 8 the advantage of InP and mHEMT technology for low noise and high gain application becomes evident.

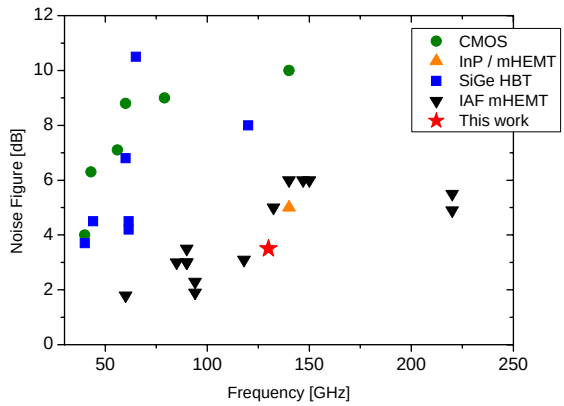

Figure 9. Noise figure of state of the art published LNAs in different semiconductor technologies.

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