Silicon nitride passivation-induced degradation in the DC and RF characteristics of 0.1-μm metamorphic high-electron-mobility transistors

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***Abstract*- We investigate effects of the Si_3N_4 passivation on the DC and RF characteristics of 0.1 μm InAlAs/InGaAs/GaAs metamorphic high-electron-mobility transistors of two different gate-recess structures. In the wide gate-recess structure, maximum drain-source saturation current ($I_{dss,max}$), maximum extrinsic transconductance ($g_{m,max}$), cut-off frequency (f_T), and maximum frequency of the oscillation (f_{max}) are reduced by 14.8, 11.6, 14.5, and 13.5%, respectively, after the passivation; on the other hand, only 5.7, 4.9, 6.6, and 7.1 % reductions are measured from $I_{dss,max}$, $g_{m,max}$, f_T, and f_{max}, respectively, in the narrow gate-recess structure. From the our modified charge control model and the simulation results based on the additional charged states present at the semiconductor/Si_3N_4, it is successfully revealed that greater degradation of DC characteristics in the wide gate-recess structure is due to the surface states of a higher density than that in the narrow gate-recess structure. A greater reduction in the f_T of the wide gate-recess structure after the passivation is also associated with the passivation-induced surface states of a higher density in the wide gate-recess structure. A greater increase of the gate-to-drain parasitic capacitance played a key role in more severe passivation-induced degradation in f_{max} of the wide gate-recess structure.**

I. INTRODUCTION

High-electron-mobility transistors (HEMTs) have been highlighted for its superior radio frequency and DC characteristics to those of conventional Si-based transistors at millimeter-wave frequencies. For example, InAlAs/InGaAs metamorphic high-electron-mobility transistors (MHEMTs) used in this study show the typical cut-off frequency and maximum frequency of oscillation of 100-440 GHz and 250-450 GHz, respectively, using the 50-100 nm gate-length technology and also exhibit the excellent low-noise performance. Due to the excellent RF and DC performance of the MHEMTs, they have promising application fields in millimeter wave systems, such as satellite or communication, radiometry, and base station.

However, similar to other semiconductor devices, the exposure of the MHEMTs to air ambient can give rise to various problems such as the degradation of the electrical performance and the physical damage through the oxidation, moisture and the pollution by dust and chemical materials. These problems critically affect the electrical characteristics of the channel layers for the two-dimensional (2D) electron transport through the exposed surface. Hence, the role of passivation is in this sense very important for device operation stability and reliability.

Silicon nitride (Si_3N_4) is one of the most common passivation materials for the GaAs MHEMT and is known to effectively protect the devices from the external damages from a conventional plasma-enhanced chemical vapor deposition (PECVD) method. However, the devices performance variation after the Si_3N_4 passivation is unavoidable, and this phenomenon is most likely associated with the surface states induced by many possible causes, such as the ion bombardment during the film deposition [1], high stress states [2], Si-NH bonding states [3].

In this study, we examined the physical role of the Si_3N_4 passivation and compared the DC and RF characteristics of the 0.1-μm MHEMTs before and after the passivation using two different gate-recess structures influencing the surface states of the device.

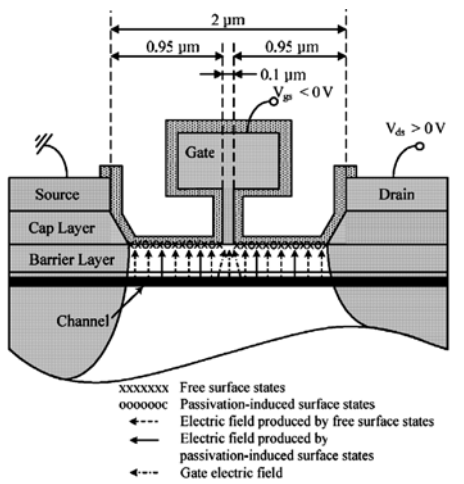
II. EXPERIMENTAL

The depletion mode MHEMT epitaxial structures were grown by molecular beam epitaxy on a semi-insulating GaAs substrate, and the overall compositions of the epitaxial structure are shown in Fig. 1. The grown epitaxial layers showed a two-dimensional electron carrier density (n_s) of ~3.5 × 10^{12} cm^{-2} and a hall mobility of ~9700 cm^2 V^{-1} s^{-1} at room temperature. To compare the DC and RF characteristics according to gate-recess structures and passivation, we fabricated the two different gate-recess structure, wide and narrow gate-recess structures has two gate fingers with a unit gate width of 70 μm, as shown in Fig. 2.

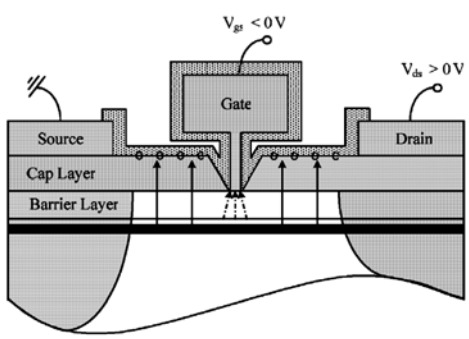
To isolate from other active regions, mesa etching was carried out by removing a 200 nm thickness in an etchant of H_3PO_4 : H_2O_2 : H_2O. Then Ohmic contacts were formed by electron beam evaporator with AuGe/Ni/Au. After metallization, rapid thermal annealing was performed at 320 ^oC for 60 sec under vacuum condition. The contact resistance showed ~3.5×10^{12} cm^{-2}. Gate-recess structures were formed by etching the cap layer with succinic acid : H_2O_2 solution. A 0.1 μm T-gate patterning was carried out by electron beam lithography system (EBPG-4HR, Leica Microsystems Ltd.) operating at an acceleration voltage of 50 keV, a beam size of

n^+ Cap Layer ($6 \times 10^{18}/cm^3$)	$In_{0.53}Ga_{0.47}As$	15 nm
i - Schottky Barrier Layer	$In_{0.52}Al_{0.48}As$	15 nm
Si delta doping ($4.5 \times 10^{12}/cm^2$)		
i - Spacer Layer	$In_{0.52}Al_{0.48}As$	3 nm
i - Channel Layer	$In_{0.53}Ga_{0.47}As$	23 nm
i - Spacer Layer	$In_{0.52}Al_{0.48}As$	4 nm
Si delta doping ($1.3 \times 10^{12}/cm^2$)		
i - Buffer Layer	$In_{0.52}Al_{0.48}As$	300 nm
i - Graded buffer Layer	$In_xAl_{1-x}As$ ($X = 0 \sim 0.5$)	1000 nm
Semi - insulating GaAs Substrate		

Fig. 1 Epitaxial structure of the MHEMT



(a)



(b)

Fig. 2 Cross-sectional schematics and effects of the electric field induced by the surface states in the cases of (a) wide and (b) narrow gate-recess structures.

50 nm and a beam current of 1 nA. After T-gate patterning, gate metal formation of Ti/Au was followed by passivating with PECVD Si_3N_4 films (80 nm) at 250 ^oC, 700 mTorr. In the case of the narrow gate-recess structure, all other process, except the gate-recess step, were performed in the same order. Gate-recess process was performed after a 0.1 μm T-gate pattering followed by descum step for stripping the remained electron beam resist in an O_2 plasma asher.

III. RESULTS AND DISCUSSION

The DC characteristics of the MHEMTs were measured in an HP 4156 DC parameter analyzer. As shown in Fig. 3, in the case of wide gate-recess structure, the maximum drain-source saturation current ($I_{dss,max}$) were ~61 and ~52 mA before and after the passivation, respectively, and maximum extrinsic transconductance ($g_{m,max}$) were ~507 and ~448 mS mm^{-1} before and after the passivation at a gate voltage (V_{gs}) of 0 V and a drain voltage (V_{ds}) of 1.5 V. In the case of the narrow gate-recess structure, $I_{dss,max}$ were ~87 and ~82 mA, and $g_{m,max}$ were ~613 and ~583 mS mm^{-1}, respectively, before and after the passivaion. The degradation of DC characteristics after the passivation has been observed in many materials systems for the HEMTs, such as InGaAs/InAlAs, GaAs/AlGaAs and InGaAs/AlGaAs. From our investigation, the degradation of DC characteristics after the passivation was much greater in the case of wide gate-recess structure.

The dependence of the DC characteristics on the gate-recess structures can be explained by the presence of the free surface states. The negatively charged free surface states on the InAlAs Schottky barrier surface decrease the channel sheet carrier density (n_s) by modulating the electric potential inside the channel. As shown in Fig. 2, the wide gate-recess structure has much greater area of exposed InAlAs surface compared to narrow gate-recess structure. The reason why the InGaAs free surface states has negligible density compared to the InAlAs surface state is not clearly understood. However, one possible cause is related to the Al-O bond on the InAlAs surface, which is observed by x-ray photoelectron spectroscopy [4]. This type of Al-O defects in the Al-alloy compound semiconductors are hardly removed because of its high thermal stability.

The area density of negatively charged free surface states (N_i) in two types of gate-recess structures with and without passivation could be estimated by using equation 1-4. The extra bias term for the effect of the negatively charged free surface states was added into the charge control model [5], and the n_s can be expressed by

$$n_s = \frac{\varepsilon_r \varepsilon_0}{e(d+\Delta d)}(V_{gs} - V_p)$$

narrow gate-recess without passivation (1)

$$n_s = \frac{\varepsilon_r \varepsilon_0}{e(d+\Delta d)}(V_{gs} - V_p - \frac{edN_p}{\varepsilon_r \varepsilon_0})$$

narrow gate-recess with passivation (2)

$$n_s = \frac{\varepsilon_r \varepsilon_0}{e(d+\Delta d)}(V_{gs} - V_p - \frac{edN_i}{\varepsilon_r \varepsilon_0})$$

wide gate-recess without passivation (3)

$$n_s = \frac{\varepsilon_r \varepsilon_0}{e(d+\Delta d)}(V_{gs} - V_p - \frac{ed(N_p + N_i)}{\varepsilon_r \varepsilon_0})$$

wide gate-recess with passivation (4)

, where ε_r is the relative dielectric constant, ε_0 is the electrical permittivity in vacuum, e is the electronic charge, d is the distance between the gate metal and the channel, Δd is the distance correction factor which is typically ~8 nm [5-7], V_p is the pinch-off voltage and N_i is the area of the free surface state, N_p is the area density of the negatively charged surface state induced by the Si_3N_4 passivation.

To validate the effects of additional charge states induced by the Si_3N_4 passivation, the hydrodynamic models simulation was performed by using the ISE TCAD simulation of

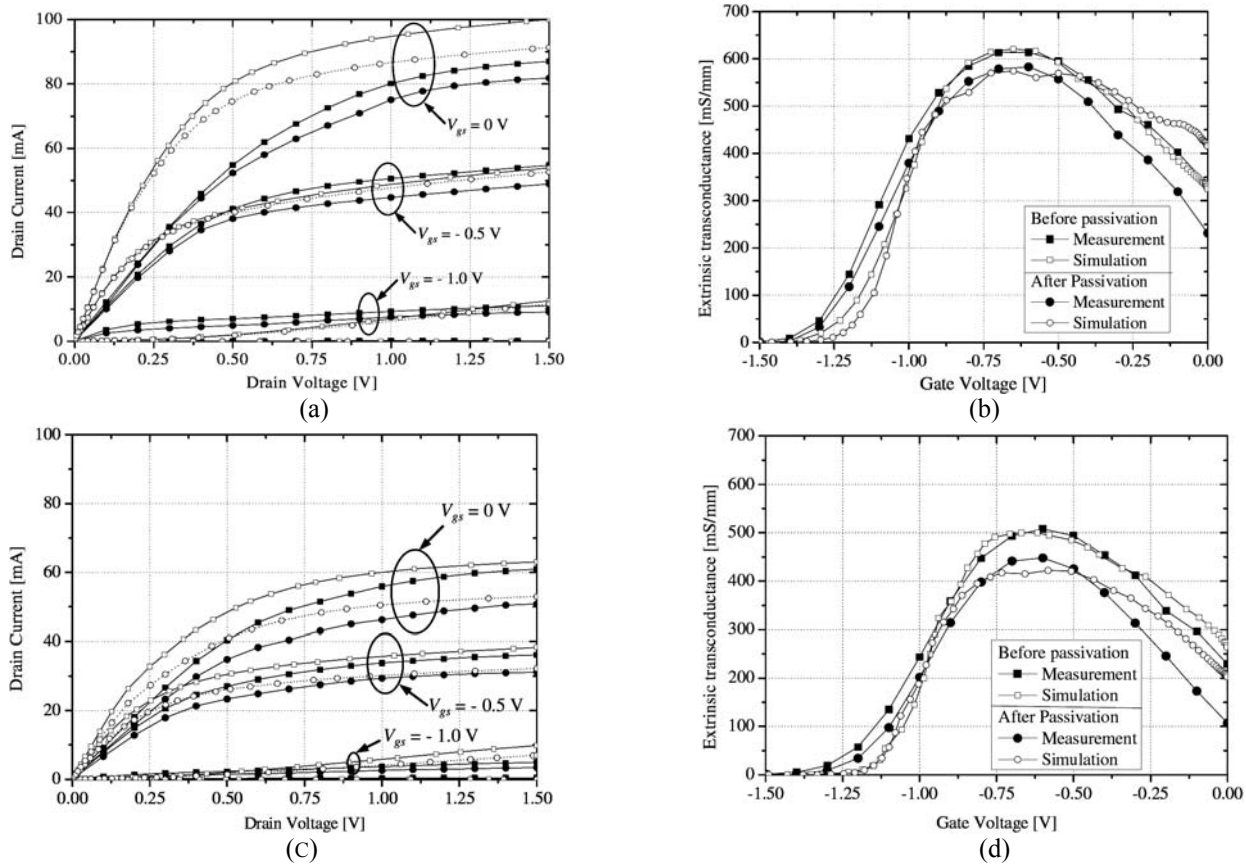


Fig. 3 Measurements and simulation results of (a) I_{ds} versus V_{ds} (b) g_m at a V_{ds} of 1 V for the narrow gate-recess structure, (c) I_{ds} versus V_{ds} (d) g_m at a V_{ds} of 1 V for the wide gate-recess structure.

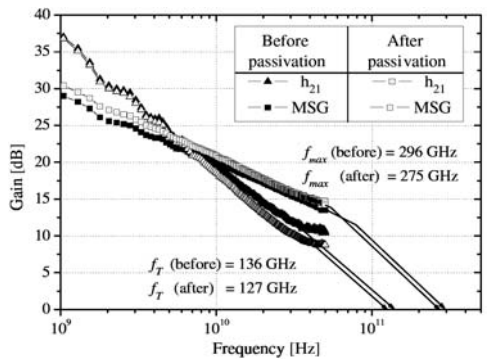
Synopysys[co] [8, 9]. For the simulation, the N_i and N_p values were estimated by using equations 1-4. The N_i value was ~1.3 × 10^{12} cm^{-2} in case of wide gate-recess structure, while no free surface state was assumed in case of narrow gate-recess. N_P values were ~1.6 × 10^{11} cm^{-2} and ~4.5 × 10^{11} cm^{-2} in cases of narrow and wide gate-recess structures, respectively. As shown in Fig. 3, the simulation results showed good agreements with the measurements and successfully supported the proposed role of surface states induced by the Si_3N_4 passivation in DC characteristics.

It is not clearly revealed yet why the wide gate-recess structures have approximately three times higher surface state density than narrow gate-recess structure. One possible explanation can be associated with the difference of contact layer of two gate-recess structures. The wide gate-recess structure undergoes various process-related damages, such as plasma-induced ion bombardment, oxidation and wet etching. The InAlAs layer exposed by wet etching can give rise to surface oxidation before the passivation because of its higher oxidation affinity than the InGaAs.

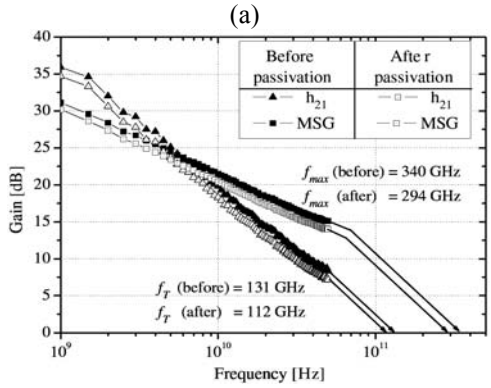
The RF characteristics were measured in a frequency range of 0.5-50 GHz using a HP 8510C network parameter analyzer. Fig. 4 are the plots of the measured maximum stable gain (MSG) and the h_{21} gain versus frequency. The f_T was defined by extrapolating the h_{21} curve at a slope of 6 dB/octave, whereas the extrapolation of the MSG curve was performed at a slope of 3 dB/octave up to a frequency where the stability factor becomes unity. As shown in Fig. 4, the narrow gate-recess structure showed less significant degradation on RF characteristics after the passivation. In the case of a wide gate-recess structure, f_T and f_{max} were ~131 and ~340 GHz, respectively, before the passivation; however, they were reduced respectively to ~112 and ~294 GHz after the passivation.

To examine the effects of the passivation on the RF characteristics, the small-signal parameters were extracted using the Dambrine method [10] as summarized in table 1, where $g_{m,int}$, C_{gs}, G_{ds}, R_i, R_s, R_g, and C_{gd} represent the intrinsic transconductance, gate-to-source capacitance, drain output conductance, intrinsic resistance, source resistance, gate resistance, and gate-to-drain capacitance, respectively. Each parameter was extracted from 12 different MHEMTs, and their average values were shown in the table 1. The f_T can be given by a relationship of $f_T \propto g_{m,int}/C_{gs}$. After the Si_3N_4 passivation, the f_T of the wide gate-recess structure exhibited a greater reduction of ~14.5 % (from 131 to 112 GHz), while the f_T of the narrow gate-recess structure was reduced by only ~6.6 % (from 136 to 127 GHz). A greater reduction of the f_T was attributed to a greater reduction of the ratio $g_{m,int}/C_{gs}$ (~10.2 %), which was originated from more severe passivation-induced degradation of the $g_{m,int}$ in the wide gate-recess structure. On the other hand, almost the same increases

in the C_{gs} were observed in both gate-recess structures. Therefore, it can be concluded that greater degradation of the f_T in wide gate-recess structure is mainly due to the passivation-induced surface states, which are more highly populated in this structure than in the narrow gate-recess structure, and the resulting degradation of the transfer characteristics.



(a)



(b)

Fig. 4 RF gains-frequency plots measured from the MHEMTs of (a) narrow and (b) wide gate-recess structures.

After the passivation, more degradation of the f_{max} was shown in the case of wide gate-recess structure. The relationships f_{max} and small-signal parameters are shown in equation (5). The f_{max} sensitively depends on the ratios $G_{ds}/g_{m,int}$ and C_{gd}/C_{gs} factors.

$$f_{\max} = \frac{f_T}{\sqrt{4\frac{G_{ds}}{g_{m,\text{int}}}(g_{m,\text{int}}R_i + \frac{R_s + R_g}{1/g_{m,\text{int}} + R_s}) + \frac{4C_{gd}}{5C_{gs}}(1 + \frac{2.5C_{gd}}{C_{gs}})(1 + g_{m,\text{int}}R_s)^2}} \quad (5)$$

As shown in table 1, the ratio C_{gd}/C_{gs} of the wide gate-recess structure produces a greater increase of ~8.5 % after the passivation than that of the narrow gate-recess structure (~3.5 %), while the ratio $G_{ds}/g_{m,int}$ shows almost the same reduction ratio in both gate-recess structures. A greater increase of C_{gd}/C_{gs} ratio in the case of wide gate-recess structure after the passivation is due to the greatest increase of C_{gd} (~15.8%) among all extracted parameters. Therefore, we can conclude that the greatest increase of C_{gd} makes a major contribution to ~13.5 % degradation of the f_{max} in the wide gate-recess structure. On the other hand, C_{gs} values are much greater than C_{gd} values in both gate-recess structures, therefore, the effect on f_{max} by the C_{gs} value was negligible.

	Narrow gate-recess structure		Wide gate-recess structure	
	Before passivation	After passivation	Before passivation	After passivation
R_g (Ω)	3.101	3.181	3.048	3.133
R_d (Ω)	5.656	5.759	5.550	5.765
R_s (Ω)	2.407	2.498	3.379	3.523
L_g (nH)	0.159	0.159	0.189	0.186
L_d (nH)	0.0960	0.0949	0.0849	0.0855
L_s (nH)	0.002 32	0.002 42	0.002 46	0.002 52
C_{pg} (pF)	0.0500	0.0528	0.0471	0.0491
C_{pd} (pF)	0.0489	0.0510	0.0459	0.0470
C_{gs} (pF)	0.0967	0.0996	0.0803	0.0835
C_{gd} (pF)	0.0122	0.0130	0.007 34	0.008 49
C_{ds} (pF)	0.0224	0.0225	0.0181	0.0183
G_{ds} (mS)	3.928	3.706	3.221	2.821
$g_{m,int}$ (mS)	80.06	78.44	63.95	59.97

Table 1 Extracted average small-signal parameters.

IV Conclusion

We investigated the effects of Si_3N_4 passivation on DC and RF characteristics of wide and narrow gate-recess structure by charge control model, and simulation based on the additional charge states present at the interface of Si_3N_4 passivation and semiconductor. From simulation results and measurement, we proposed that the greater degradation of DC characteristics and f_T in the wide gate-recess structure was due to the surface states of higher than that of narrow gate-recess structure. But, the degradation of f_{max} was due to gate-to-drain parasitic capacitance induced by Si_3N_4 passivation.

Acknowledgment

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