Low noise amplifiers for G-band radiometers

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***Abstract*-Six low noise amplifiers (LNAs) for three frequency ranges are presented. The amplifier circuits have been manufactured using a 100-nm gate length metamorphic high electron mobility transistor technology. Measured on-wafer performance shows 19-27 dB of gain and lowest noise figure values of 4 dB.**

I. Introduction

The advances in semiconductor technologies for millimeter-wave monolithic integrated circuits (MMICs) have made use low noise amplifier possible for higher frequency, namely up to 500 GHz [1]. For spaceborne radiometry above 140 GHz two main benefits of low noise amplifiers can be foreseen. First benefit is low-noise pre-amplification in front of currently used radiometers based on Schottky mixers improving receiver sensitivity. Secondly, low noise amplifiers enable the use of direct-detection radiometers.

II. Fabrication Technology

The manufacturing of low noise millimetre-wave integrated circuits has traditionally relied to use of high electron mobility transistors (HEMT) implemented with gallium arsenide (GaAs) or indium phosphide (InP). The best results have been achieved with InP technology. However, there are some drawbacks with the InP technology. These include higher manufacturing cost, lower breakdown voltage, more fragile structure, and device reliability when comparing to GaAs technology. To overcome some of these drawbacks, the possibility to process InP channel devices on the GaAs carrier wafer have been introduced in pseudomorphic (PHEMT) and metamorphic (MHEMT) technologies. In MHEMT technology, the metamorphic buffer layer is grown on the GaAs substrate, to enable the growth of the channel layer having 30-80 % indium content. This leads to cost reduction and manufacturability improvement over pure InP technology. The process can also be optimised for the intended purpose by controlling the indium content. The higher indium content provides more gain and less noise, whereas lower indium content is more suitable for applications requiring higher breakdown voltage [2].

The manufacturing process used in this work is the 100-nm GaAs based MHEMT technology of the Fraunhofer IAF, Freiburg, Germany. The process is suitable for coplanar waveguide (CPW) designs. The process features NiCr thin film resistors, metal-insulator-metal (MIM) capacitors and backside metallization. Unwanted substrate modes are suppressed using ground via holes through the GaAs substrate. As a result of extensive modelling work the Fraunhofer IAF provided reliable models for CPW components and transistors [3]. On-wafer G-band measurements of the test devices for the models suffered from serious systematic experimental errors, which were observed at the IAF as well as at Millilab. This phenomenon was attributed to an interference of the probe-tips with the neighboring on-wafer circuitry and is presently under detailed investigation. It impeded the extension of the model data base to G-band frequencies. Unfortunately, some parasitic and distributed effects become visible only at frequency above 100 GHz and lead to an unpredicted shift of up to 10 GHz to lower frequencies in the realized MMICs.

III. Designs and Measured Performance

Six low noise amplifiers were designed. LNA1 and LNA2 were targeted to narrowband operation at 165 ± 2 GHz, LNA3, LNA4, and LNA5 for a wide frequency range over 183 ± 10 GHz, and LNA6 for narrowband operation at 229 ± 2 GHz. Design goal was 20 dB of gain with -10 dB input and output match while achieving low noise performance.

All designs use coplanar waveguide (CPW) topology. Transistors with gate widths of 2x10 µm and 2x15 µm were chosen for the LNAs. Larger transistor was used for 165 GHz and smaller transistor for the two higher frequency ranges. Transistors achieve peak transconductance with 400 mA/mm drain current density and f_t is around 220 GHz. Availability of noise model enabled noise optimised designs.

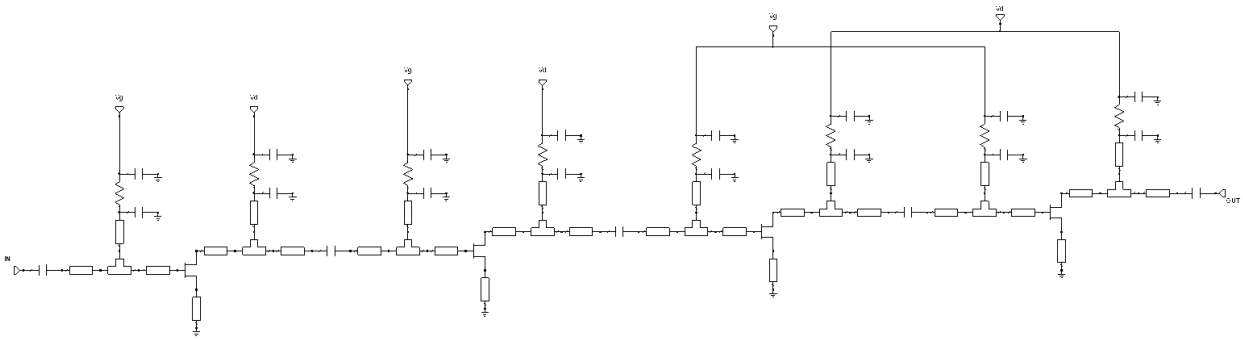

Figure 1. Schematics for baseline LNA design.

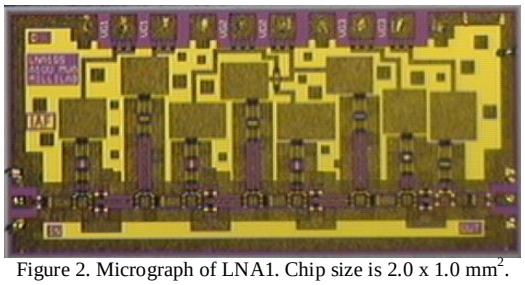

Figure 2. Micrograph of LNA1. Chip size is 2.0 x 1.0 mm^2.

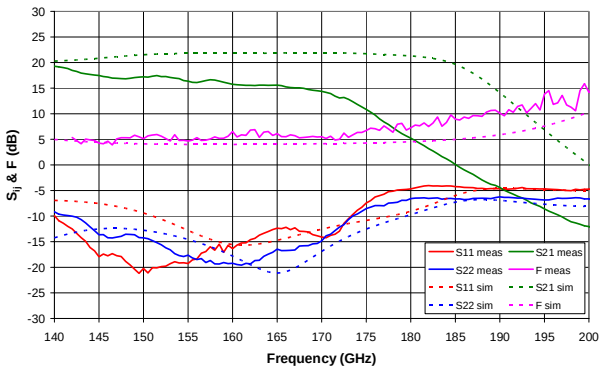

Figure 3. Measured (solid) and simulated (dashed) performance of LNA1.

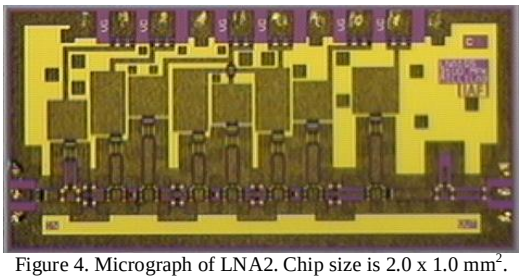

Figure 4. Micrograph of LNA2. Chip size is 2.0 x 1.0 mm^2.

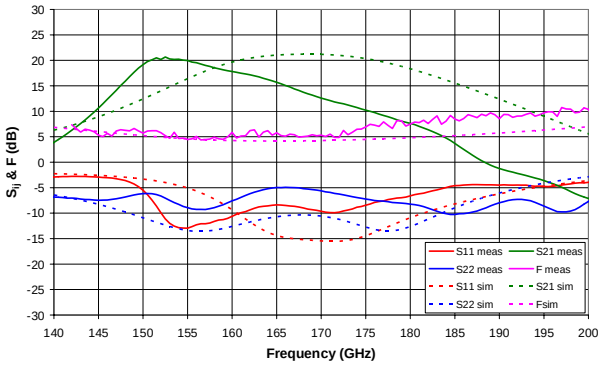

Figure 5. Measured (solid) and simulated (dashed) performance of LNA2.'

Schematics for a baseline LNA design is presented in Fig. 1. Matching networks are realised with conventional reactive matching networks, consisting of series transmission lines, series capacitors, and RF-short circuited shunt stubs. RF-short is realised using appropriately valued CPW-capacitor, typically 200-400 fF. Shunt stubs are used also for biasing. Low frequency stability is improved by small valued resistor and large MIM-capacitor following the RF-shorting capacitor on bias lines. Stability is further improved by using inductive source feedback.

A. LNA1

LNA1 is a 4-stage design using 2x15 µm transistors. Wideband approach to design was selected to mitigate possible frequency shifts. Micrograph of the circuits is shown in Fig. 2. The stages are biased below peak transconductance current density to improve stability. Second RF-shorting capacitor is added between series resistor and MIM-capacitor. Otherwise, design follows the baseline.

Comparison of measured and simulated S-parameters and noise figure is presented in Fig. 3. The measured gain and noise figure are 15.5 dB and 5.9 dB at 165 GHz, respectively. The best gain and noise performance is achieved around 140 GHz, where gain of 19.8 dB and noise figure of 5.0 dB are reached. The input and output matches are better than -10 dB over 136-174 GHz and 132-174 GHz, respectively.

B. LNA2

LNA2 is a narrowband 4-stage design using 2x15 µm transistors. The design was targeted for 165 GHz center frequency. Micrograph of LNA2 is shown in Fig. 4. The stages are biased below peak transconductance current density to improve stability. Design follows the baseline with an additional open ended stub that is added on output matching network to obtain wider bandwidth for matching.

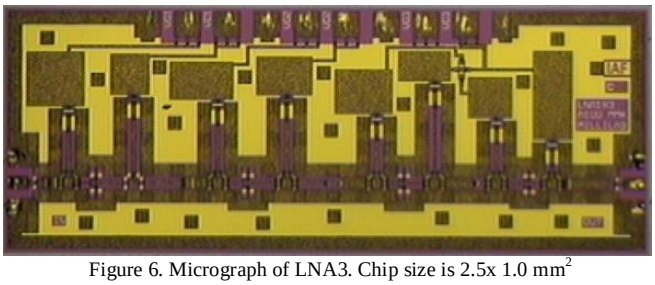

Figure 6. Micrograph of LNA3. Chip size is 2.5x 1.0 mm^2

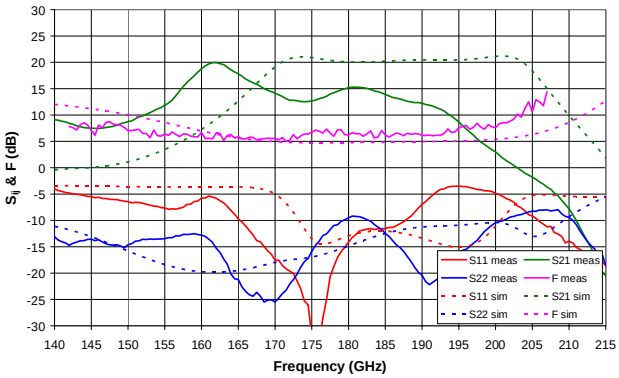

Figure 7. Measured (solid) and simulated (dashed) performance of LNA3.

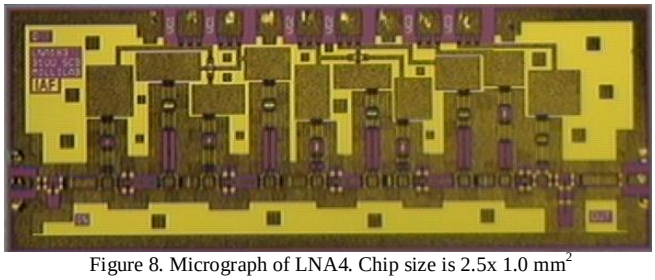

Figure 8. Micrograph of LNA4. Chip size is 2.5x 1.0 mm^2

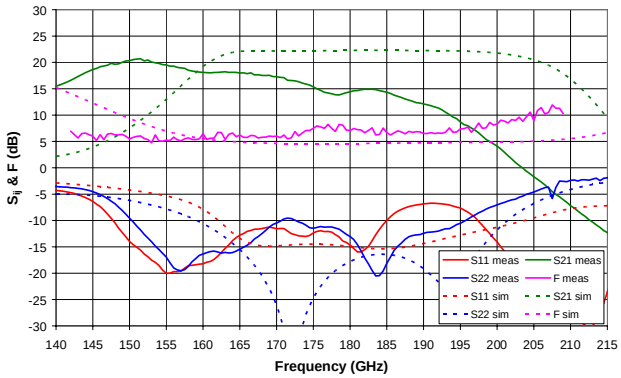

Figure 9. Measured (solid) and simulated (dashed) performance of LNA4.

Comparison of measured and simulated S-parameters and noise figure is presented in Fig. 5. The peak gain of 20.5 dB is achieved at 153 GHz and minimum noise of 4.3 dB at 156 GHz. The input and output matches are worse than simulated. The output match is better than -5 dB over 140-200 GHz and the input match reaches -10 dB level almost over 152-174 GHz.

C. LNA3

LNA3 is a wideband 4-stage design using 2x10 µm transistor. The stages are biased to peak transconductance current density. Realisation follows the baseline design. Micrograph of LNA3 is shown in Fig. 6.

The comparison of measured and simulated S-parameters and noise figure is presented in Fig. 7. The peak gain of 20 dB is achieved at 163 GHz and minimum noise of 5.3 dB at 172 GHz. The output match is better than -10 dB over 140-202 GHz and the input match is better than -10 dB level almost over 166-187 GHz.

D. LNA4

LNA4 is a wideband 5-stage design using transistors sizes in between 2x10 µm and 2x12 µm. Micrograph of LNA4 is shown in Fig. 8. Stages 1 and 2 are biased below peak transconductance current density, while stages 3, 4 and 5 are biased to peak transconductance current density. Main difference to design baseline is an additional 5th stage, which gives margin for gain per stage requirement. Also, open ended shunt stubs are added to input and output matching networks.

Comparison of simulated small-signal and noise performance is presented in Fig. 9. The best operation is achieved around 150 GHz, where gain of 20.2 dB and noise figure of 5.0 dB are measured. At 183 GHz are obtained 14.9 dB gain and 7.5 dB noise figure. Input and output matches remain below -10 dB over 148-184 GHz and 151-196 GHz, respectively.

E. LNA5

LNA5 is a five stage amplifier using 2x10µm transistors. Micrograph of the design is shown in Fig. 10. First three stages are biased below peak transconductance current density for better noise performance. Fourth and fifth stages are biased for peak transconductance current density. Additional fifth stage is added to the baseline design and capacitively loaded T-junctions are used in matching networks.

Comparison of measured and simulated S-parameters and noise figure at this bias point is presented in Fig. 11. This leads to gain peaking at 157 GHz where gain is reaching 29.0 dB. Also, input and output match are poor here and only conditional stability is achieved. Otherwise, the output match is better than -10 dB over 163-184 GHz and the input match reaches -10 dB over 180-187 GHz. Noise curve has quite nice and flat shape and values below 6 dB are reached between 166-173 GHz.

F. LNA6

LNA6 is a four stages design using 2x10 µm transistors. Micrograph of the design is shown in Fig. 12. All stages are biased to peak transconductance bias point and design follows the baseline design.

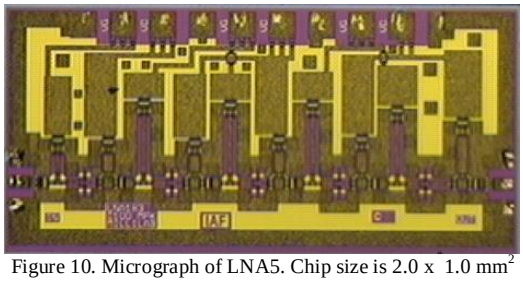

Figure 10. Micrograph of LNA5. Chip size is 2.0 x 1.0 mm^2

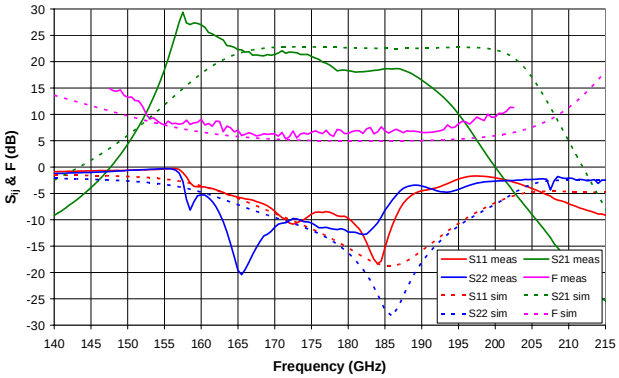

Figure 11. Measured (solid) and simulated (dashed) performance of LNA5.

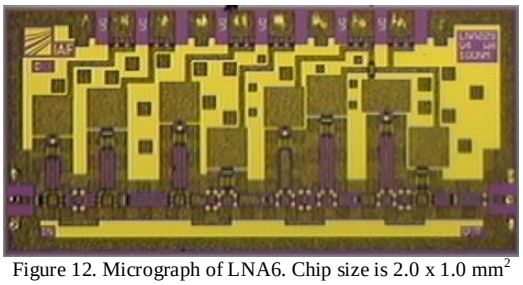

Figure 12. Micrograph of LNA6. Chip size is 2.0 x 1.0 mm^2

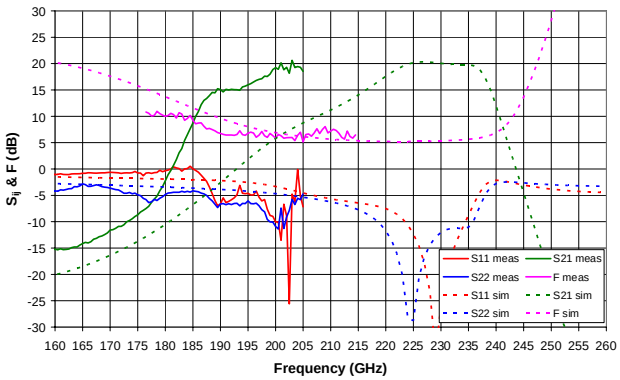

Figure 13. Measured (solid) and simulated (dashed) performance of LNA6.

TABLE I
MEASURED ON-WAFER PERFORMANCE OF THE DESIGNED AMPLIFIERS

Circuit	-3 dB Gain band (GHz)	Peak gain (dB)	< -10 dB Input match (GHz)	< -10 dB Output match (GHz)	Noise figure (dB)	Power consumption (mW)
LNA1	140-159	19.2	140-173	142-173	3.9-5.9	40
LNA2	149-160	20.6	152-161	N.A.	4.3-6.3	40
LNA3	158-166	19.9	165-188	140-179	5.4-6.8	35
LNA4	143-167	20.7	180-186	163-184	4.4-5.9	40
LNA5	157-161	27.4	171-174	163-184	8.2-9.5	37
LNA6	199-207	20.2	200-201	199-201	5.4-7.1	32

Comparison of measured and simulated S-parameters and noise figure at this bias point is presented in Fig. 13. Peak gain of 20 dB and minimum noise figure of 5.5 dB are achieved at 205 GHz. The input is very close to 0 dB at 183 GHz and reaches -10 dB on a narrow band around 201 GHz. The output match reaches also -10 dB on a narrow band near 200 GHz.

IV. CONCLUSIONS

Summary of measured performance is presented in Table I. Frequency shift in gain response was observed for all amplifier designs. Further investigations showed that the frequency shift could be attributed to the incomplete descriptions of the source line connection parasitics and a distributed effect in the parallel capacitors.

Gain values of 20 dB and noise figure values of 4-5 dB were achieved for the amplifiers, with one exception related to unstable operation. With the results from the first run amplifiers could be re-designed to obtain better performance over the targeted bands.

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